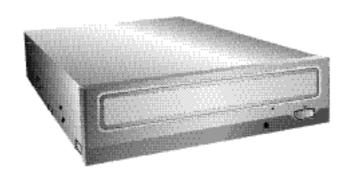


Super Multi DVD Drive SERVICE MANUAL

MODEL: GSA-4165B/

GSA-4167B/

GSA-4168B



P/NO: 3828HS1047G

August 2005 Printed in Korea

MODEL: GSA-4165B/GSA-4167B/GSA-4168B

TABLE OF CONTENTS

INTRODUCTION	
FEATURES	
SPECIFICATIONS	
LOCATION OF CUSTOMER CONTROLS	
DISASSEMBLY	
1. CABINET and CIRCUIT BOARD DISASSEMBLY	
1-1. Bottom Chassis	12
1-2. Front Bezel Assy	12
1-3. Cabinet and Main Circuit Board	12
2. MECHANISM ASSY DISASSEMBLY	12
2-1. Pick-up Unit	12
2-2. Pick-up	13
EXPLODED VIEW	
MECHANICAL REPLACEMENT PARTS LIST	16~18
GLOSSARY	
THE DIFFERENCES OF CD-R/CD-RW DISCS AND GENERAL CD-ROM	
1. Recording Layer	
2. Disc Specification	
3. Disc Materials	21
4. Reading Process of Optical Disc	22
5. Writing Process of CD-R Disc	
6. Writing Process of CD-RW Disc	
7. Organization of the PCA, PMA and Lead-in Area	
8. Function of PCA and PMA area	
9. OPC and ROPC	
10. Writing Process of DISC	
THE DIFFERENCES OF DVD-R/RW, DVD+R/RW DISCS AND DVD-ROM	
1. Recording Layer	
2. Disc Specification	
3. Disc Materials	
4. Writing Pulse Waveform of DVD+R	
5. Writing Pulse Waveform DVD+RW	
6. Organization of Inner Drive Area, Outer Drive Area, Lead-in Zone and Lead-out Zone	
LightScribe MEDIA	
1. LightScribe Media	
Hardware Block Diagram of LightScribe Label Printing MR Assay Fact Light Oscillar.	
3. MD Assy For LightScribe	
4. Optical Encoder Assy	
DVD & CD DATA PROCESSING	
Copy Protection and Regional Code Management Block	
3. About Prevention the DVD-ROM from to be copy	
4. About the DVD-ROM Regional Code	
1. Block Diagram of the Pick-up(HOP-7632TS)	
Pick up Pin Assignment Signal detection of the P/U	
DESCRIPTION OF CIRCUIT	
1. ALPC Circuit	
2. Focus Circuit	
3. Tracking & Sled Circuit	
4. Spindle Circuit	
MAJOR IC INTERNAL BLOCK DIAGRAM AND PIN DESCRIPTION	
TROUBLESHOOTING GUIDE	
BLOCK DIAGRAM	
PRINTED CIRCUIT BOARD DIAGRAM	
ELECTRICAL REPLACEMENT PARTS LIST	

INTRODUCTION

This service manual provides a variety of service information.

It contains the mechanical structure of the Super Multi DVD Drive and the electronic circuits in schematic form. This Super Multi DVD Drive was manufactured and assembled under our strict quality control standards and meets or exceeds industry specifications and standards.

This Super Multi DVD drive is an internal drive unit designed for use with IBM PC, HP Vectra, or compatible computer. It can write as much as 700 Mbytes of digital data into CD-R/RW disc, and can read as much as 700 Mbytes of digital data stored in a CD-ROM/R/RW disc.

It can write as much as 4.7Gbytes of digital data into DVD-R/RW/RAM/+R/+RW disc, and can read as much as 4.7Gbytes of digital data stored in a DVD-ROM/R/RW/RAM/+R/+RW disc.

It can write as much as 8.5Gbytes of digital data into DVD+R DL/DVD-R DL disc, and can read as much as 8.5Gbytes of digital data stored in a DVD-ROM DL/+R DL/-R DL disc.

This Super Multi DVD Drive can easily meet the upcoming MPC level 3 specification, and its Enhanced Intelligent Device Electronics (E-IDE) and ATAPI interface allows Plug and play integration in the majority of today's PCs without the need of an additional interface card.

1. Support feature and writable disc

*) Indicated write-in speed is a value at the time of the fastest operation.

			G*A-4165B			
	GSA	GMA	GWA	GRA	GCA	GDA
Light Scribe	Х	х	Х	Х	Х	Х
CD-R	48x write	read only				
CD-RW	32x write	read only				
DVD-R	16x write	16x write	16x write	read only	16x write	16x write
DVD-RW	4x or 6x write	4x or 6x write	4x or 6x write	read only	4x or 6x write	4x or 6x write
DVD-R DL	4x write	4x write	4x write	read only	4x write	4x write
DVD+R	16x write	read only	16x write	16x write	read only	read only
DVD+RW	8x write	read only	8x write	8x write	read only	read only
DVD+R DL	4x or 6x write	read only	4x or 6x write	4x or 6x write	read only	read only
DVD-RAM	5x write	5x write	read only	read only	read only	5x write

			G*A-4167B			
	GSA	GMA	GWA	GRA	GCA	GDA
Light Scribe	X	x	x	x	X	X
CD-R	48x write	read only				
CD-RW	32x write	read only				
DVD-R	16x write	16x write	16x write	read only	16x write	16x write
DVD-RW	6x write	6x write	6x write	read only	6x write	6x write
DVD-R DL	4x write	4x write	4x write	read only	4x write	4x write
DVD+R	16x write	read only	16x write	16x write	read only	read only
DVD+RW	8x write	read only	8x write	8x write	read only	read only
DVD+R DL	6x write	read only	6x write	6x write	read only	read only
DVD-RAM	5x write	5x write	read only	read only	read only	5x write

			G*A-4168B			
	GSA	GMA	GWA	GRA	GCA	GDA
Light Scribe	0	0	0	0	0	0
CD-R	48x write	read only				
CD-RW	32x write	read only				
DVD-R	16x write	16x write	16x write	read only	16x write	16x write
DVD-RW	6x write	6x write	6x write	read only	6x write	6x write
DVD-R DL	4x write	4x write	4x write	read only	4x write	4x write
DVD+R	16x write	read only	16x write	16x write	read only	read only
DVD+RW	8x write	read only	8x write	8x write	read only	read only
DVD+R DL	6x write	read only	6x write	6x write	read only	read only
DVD-RAM	5x write	5x write	read only	read only	read only	5x write

FEATURES

1 General

- 1) Enhanced IDE (ATAPI) interface.
- 2) Internal Half-height Drive.
- 3) CD-R/RW, DVD-R/-R DL(Dual Layer)/-RW/RAM/+R/+R DL(Double Layer)/+RW read and write compatible CD Family and DVD-ROM read compatible.
- 4) Buffer Under-run prevention function embedded.
- 5) 2MB buffer memory.
- 6) Power loading and power eject of a disc. Bare media loading.
- 7) MTBF: 100,000 POH
- 8) Vertical and Horizontal installable.

2. Supported disc formats

- 1) Reads data in each DVD-ROM, DVD-R(Ver. 2.0 for Authoring) and DVD-RAM(Ver.1.0)
- 2) Reads and writes in each DVD-R(Ver. 2.0 for General), DVD-R DL(Dual Layer), DVD-RW, DVD-RAM(Ver.2.2), DVD+R, DVD+R DL(Double Layer) and DVD+RW
- 3) Reads data in each CD-ROM, CD-ROM XA, CD-I, Video CD, CD-Extra and CD-Text
- 4) Reads data in Photo CD (Single and Multi session)
- 5) Reads standard CD-DA
- 6) Support to read Super Audio CD(Compatible layer in Hybrid type)
- 7) Reads and writes CD-R discs conforming to "Orange Book Part 2"
- 8) Reads and writes CD-RW discs conforming to "Orange Book Part 3"
- 9) Reads DVD-RAM with CPRM and DVD-RW with CPRM

3. Supported write method

• •	
1) DVD-R:	Disc at Once and Incremental Recording
2) DVD-R DL	Disc at Once, incremental Recording and Layer jump recording
3) DVD-RW:	Disc at Once, Incremental Recording and Restricted Overwrite
4) DVD-RAM:	Random Write
5) DVD+R:	Sequential Recording
6) DVD+R DL:	Sequential Recording
7) DVD+RW:	Random Write

8) CD-R/RW:Disc at Once, Session at Once, Track at Once and Packet Write

4. Performance

1) Average access time: DVD-ROM 145 ms (1/3 stroke) CD-ROM 125 ms

2) Write speed: DVD-R 2x, 4x CLV, 8x ZCLV, 16x PCAV

DVD-R DL 2x, 4x CLV

DVD-RW 1x, 2x, 4x, 6x CLV

DVD-RAM 2x, 3x ZCLV (Ver.2.2), 3x-5x PCAV(Ver.2.2) DVD+R 2.4x, 4x CLV, 8x ZCLV, 12x, 16x PCAV

DVD+R DL 2.4x, 4x, 6x CLV DVD+RW 2.4x, 4x CLV, 8x ZCLV

CD-R 4x, 8x, 16x CLV, 24x, 32x, 40x, 48x ZCLV

CD-RW 4x, 10x, 16x CLV, 24x, 32x ZCLV

(High Speed: 10x, Ultra Speed: 16x, 24x, 32x)

3) Read speed: DVD-R/RW/ROM/ROM-Dual layer 10x / 8x / 16x / 12x max.

DVD-R DL 8x max.

DVD-RAM (Ver.1.0/2.2) 2x / 2x, 3x ZCLV, 3x-5x PCAV DVD-Video(CSS Compliant Disc) 8x max. (Single/Dual layer)

DVD+R/+RW 10x / 8x max. DVD+R DL 8x max.

CD-R/RW/ROM 48x/40x/48x max.

CD-DA (DAE) 40x max. 80mm CD 16x max.

4) Sustained Transfer rate: DVD-ROM 22.16 Mbytes/s (16x) max.

CD-ROM 7,200 kB/s (48x) max.

5) Burst Transfer rate: Ultra DMA Mode2

Multi word DMA Mode2, PIO Mode 4

6) Multimedia MPC-3 compliant

5. Audio

- 1) 16 bit digital data output through ATA interface
- 2) Software Volume Control
- 3) Equipped with audio line output for audio CD playback

*Definition

Transfer Rate:1x (DVD) = 1.385 Mbytes/s.....1x (CD) = 150 kB/s Mbytes/s = 10^6 bytes/s,kB/s = 2^{10} bytes/s

Capacity:MB = 2²⁰ bytes,kB = 2¹⁰ bytes

SPECIFICATIONS

1. SYSTEM REQUIREMENTS

-CPU: IBM Compatible Pentium 4 2.4GHz (or faster)

(For High speed, 2.4GHz or faster recommended.)

-128MB Memory or greater

2. SUPPORTING OPERATING SYSTEM

* Operating System

Windows Millennium Edition (Me)

Window 2000 Professional (2) In CD(Ahead)

Window XP Home Edition, Professional

(3) Power Producer Gold (Cyber Link)

2.1 Applicable disc formats

4.7GB (Single Layer) DVDDVD-ROM:

8.5GB (Dual Layer)

* Recording tool

(1) Nero(Ahead)

DVD-R DL: 8.5GB

4.7GB (Ver.2.0 for Authoring : read only) DVD-R:

4.7GB (Ver.2.0 for General: read & write)

DVD-RW: 4.7GB (Ver.1.2) DVD-RAM: 2.6GB/side (Ver.1.0)

1.46GB/side, 4.7GB/side (Ver.2.2)

DVD+R: 4.7GB DVD+R DL: 8.5GB DVD+RW: 4.7GB

CD......CD-ROM Mode-1 data disc

CD-ROM Mode-2 data disc

CD-ROM XA, CD-I, Photo-CD Multi-Session, Video CD

CD-Audio Disc

Mixed mode CD-ROM disc (data and audio)

CD-Extra **CD-Text**

CD-R (Conforming to "Orange Book Part2": read & write) CD-RW (Conforming to "Orange Book Part3": read & write)

2.2 Writing method

(1) DVD-R/RWDisc at Once

Incremental Recording

Restricted Overwrite (DVD-RW only)

(2) DVD-R DLDisc at Once

Incremental Recording Layer jump Recording

(3) DVD-RAM/+RWRandom Write

(4) DVD+RSequential Recording (5) DVD+R DLSequential Recording

(6) CD-R/RWDisc at Once (DAO)

Session at Once (SAO)

Track at Once (TAO)

Packet Write

2.3 Disc diameter......120mm

80mm (Horizontal only)

2.4 Data capacity

DVD-ROM/R/RW/RAM/+R/+RW2,048 bytes/block User Data/Block

CD (Yellow Book)2,048 bytes/block(Mode 1 & Mode 2 Form 1)

2,336 bytes/block (Mode 2)

2,328 bytes/block (Mode 2 Form 2)

2x 4x(CLV) 8x(7CLV) 16x(PCAV)

2,352 bytes/block (CD-DA)

2.5 RPC (Regional Playback Control) Phase2, No Region

3. DRIVE PERFORMANCE

<Write>

3.1 Host interface	X3T13 ATA/ATAPI5/1321D
	INF-8090i Rev.5.3

3.2 Read/Write & Rotational speed DVD-R

	2x, +x(OLV), Ox(2OLV), TOX(1 O/TV)
DVD-R DL	2x, 4x(CLV)
DVD-RW	1x, 2x, 4x, 6x(CLV)
DVD-RAMVer. 2.2	2x, 3x(ZCLV), 3x-5x(PCAV)
DVD+R	2.4x, 4x(CLV), 8x, 12x, 16x(PCAV)
	DVD-R DL

DVD+R DL2.4x, 4x, 6x(CLV)

DVD+RW......2.4x, 4x(CLV), 8x(ZCLV)

CD-R4x, 8x, 16x(CLV), 24x, 32x, 40x, 48x(ZCLV)

CD-RW4x, 10x,16x(CLV), 24x, 32x (ZCLV)

(High Speed: 10x, Ultra Speed: 16x, 24x, 32x)

DVD-ROM......Single layer......6.7x - 16x (CAV), Approx. 9,420 r/min <Read>

> DVD-R DL8.5GB3.3x - 8x (CAV), Approx 5,180r/min DVD-R......4.7GB4.2x - 10x (CAV), Approx. 5,890 r/min

DVD-RAMVer. 1.0/ 2.22x/ 2x, 3x (ZCLV)* 3x-5x (PCAV)*

DVD+R......4.7GB4.2x - 10x (CAV), Approx. 5,890 r/min DVD+R DL8.5GB3.3x - 8x (CAV), Approx. 5,180 r/min

DVD+RW4.7GB3.3x - 8x (CAV), Approx. 4,720 r/min

CD-R/ROM, CD-I / Video(1.2m/s)20x - 48x (CAV), Approx. 9,540 r/min

CD-RW(1.2m/s)16.7x - 40x (CAV), Approx. 8,100 r/min CD-DA (DAE).....(1.2m/s)16.7x - 40x (CAV), Approx. 8,100 r/min

CD-DA (Audio out)(1.2m/s)4.0x - 10x (CAV), Approx. 2,030 r/min

* Rotational speed (CLV, ZCLV)

DVD-R/RW/ROM, +R/RW1x: Approx. 1,390(Inside) - 580 r/min(Outside) DVD-RAM.......Ver. 1.01x: Approx. 2,390(Inside) - 1,010 r/min(Outside) Ver. 2.22x: Approx. 3,250(Inside) - 1,380 r/min(Outside)

	ransfer rate stained transfer rate		
<write></write>	DVD-R	.2.77, 5.54, 5.44-11.08 Mbytes/s	2x, 4xCLV, 8x ZCLV
		9.14-22.16 Mbytes/s	
	DVD-R DL	.2.77, 5.54 Mbytes/s	
	DVD-RW	.1.385, 2.77, 5.54, 8.31 Mbytes/s	1x, 2x, 4x, 6x CLV
		.2.77, 4.15, 4.15-6.925 Mbytes/s (w/o Verify)	
		.3.32, 5.54, 8.31-11.08 Mbytes/s	
		8.31-16.62, 9.14-22.16 Mbytes/s	12x ZCLV, 16x PCAV
	DVD+R DL	.3.32, 5.54, 8.31 Mbytes/s	2.4x, 4x, 6x CLV
	DVD+RW	.3.32, 5.54, 8.31-11.08 Mbytes/s	2.4x, 4x CLV, 8x ZCAV
	CD-R	.600, 1,200, 2,400, 2,400-3,600, 2,400-4,800, 2,400-6,0	
	CD-RW	.600, 1500, 2,400, 2,400- 3,600, 2,400-4,800 k	B/s (Mode-1)
4Boods	DVD BOM	.Single layer9.28 - 22.16 Mbytes/s	
<reau></reau>		.Dual layer6.86 - 16.62 Mbytes/s	
		5.73 - 13.85 Mbytes/s5.73	
		4.58 - 11.08 Mbytes/s	
		4.58 - 11.08 Mbytes/s	
		.Ver. 1.02.77 Mbytes/s	
		.Ver. 2.22.77, 4.155,4.155-6.93 Mbytes/	
		5.73 - 13.85 Mbytes/s	
		4.58 - 11.08 Mbytes/s	
		4.58 - 11.08 Mbytes/s4.58 - 11.08 Mbytes/s	
		3,000 - 7,200 kB/s	
		2,500 - 6,000 kB/s	
		2,500 - 6,000 kB/s	
3 3 2 Rui	rst transfer rate	2,300 - 0,000 KB/S	40x IIIax.
3.3.2 Dui		33.3 Mbytes/s max.	
		216.6 Mbytes/s max.	
		16.6 Mbytes/s max.	
3 4 Acces	s time (1/3 stroke)	10.0 Mbytes/3 max.	
0.4 A0003	•	145 ms Typ.* (Note 1)	
		165 ms Typ.	
	,	125ms Typ. (Note 1)	
Note:		,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	
1) Average	random access time is the	typcal value of more than 50 times including latence	y and error correction time.
	Test Disc : DVD : A	LMEDIO TDV-520 / TDR-820	
	CD : Al	MEDIO TCDR-701 / HITACHI HCD-1	
*) Typical va	alue defines a measured v	ralue in normal temperature (20 deg.C.) and horizon	ntal position.
3.5 Data e	rror rate (Measured wi	th 5 retries maximum)	
	•	/RAM<10 ⁻¹²	
	DVD+R/+RW	<10 ⁻¹²	

DVD+R/+RW.....<10-CD-R/RW/ROM.....<10⁻¹² (Mode-1) <10⁻⁹ (Mode-2)

Condition : It is assumed that the worst case raw error rate of the disc is 10°

3.6 Data buffer capacity2 Mbytes

4. Quality and Reliability

4.1 MTBF	100,000 Power On Hours(Consecutive/Cumulative POH)
Assumption:	Used in a normall office environment at room temperature.
-POH per year	3,000
-ON/OFF cycles per year	600
-Operating duty cycle	20% of power on time (Seek: 5% of operating time)
4.2 Tray cycle test	30,000 times
	No degeneration in the mechanical part after test
4.3 Actuator mechanism	1,000,000 full stroke seek
4.4 MTTR (Mean Time To Repair)	0.5 h
4.5 Component life	5 years or 2,000 h of Laser radiating time
Assumption:	Used in a normall office environment.

5. POWER REQUIREMENTS

5.1 Source voltage

+5V ± 5% tolerance, less than 100 mVp-p Ripple voltage

+12V ± 10% tolerance, less than 100 mVp-p Ripple voltage

5.2 Current

+5V DC	0.9A typ	< 1.0 A max.
+12V DC	0.5A typ	< 1.0 A max.
+5V DC	1.3A typ	< 1.5 A max.
+12V DC	0.9A typ	< 1.5 A max.
+5V DC	1.0A typ	< 1.5 A max.
+12V DC	0.9A typ	< 1.5 A max.
+5V DC	1.0A typ	< 1.5 A max.
+12V DC	1.2A typ	< 2.0 A max.
	+12V DC +5V DC +12V DC +5V DC +12V DC	.+5V DC

5.3 Standby

Sleep mode (No disc)1.1 W typ. 1.3 W max.

6. AUDIO PERFORMANCE

Output Level (1kHz, 0dB)	0.7 Vrms typical
Frequency Response	+/-3dB (20 to 20,000Hz)
Signal to Noise Ratio	80 dB min. with IHF A and LPF 20 kHz
THD (1kHz, 0dB)	0.10% max. with LPF 20 kHz
Channel separation(10kHz)	65 dB min.
Condition:	Load inpedance : 10 kohms

7. Acoustic noise

Less than 50dB, A scale, at 0.5 m away from the drive

Note: 1. Disc: Less than imbalance 0.3 x 10⁻⁴ Nm

2. Installation: Horizontal

3. Ambient temperature: Normal temperature

4. Except loading, unloading and seek

8. Dimensions

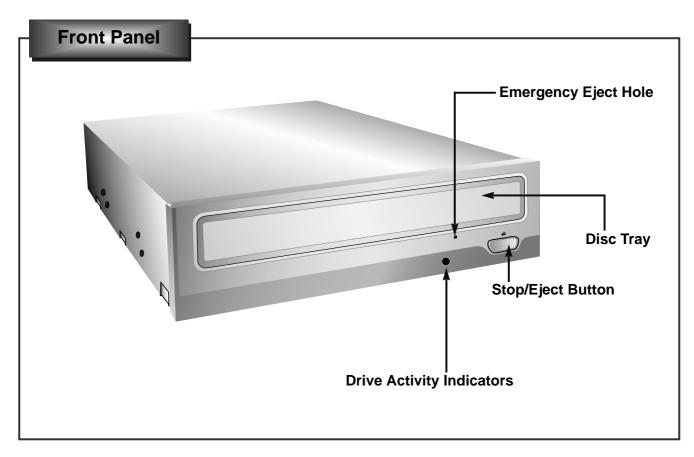
External dimensions (W x H xD) 146 x 41.3 x 165mm(without Bezel)

Front bezel (WxHxD) 148 x 42 x 5 mm

9. MassApprox. 0.77+/-0.03 kg

^{*} Which is not provided with Circuit Diagram of this model. Please Contact the friendly staff of LG Service Care at: Website http://www.LGEservice.com

LOCATION OF CUSTOMER CONTROLS



1. Disc tray

This is the tray for the disc. Place the disc on the ejected disc tray, then lightly push the tray (or push the eject button) and the CD will be loaded.

NOTE: Don't pull out or push in the disc tray forcibly. This might cause damage to the loading section of the drive.

2. Stop/Eject button

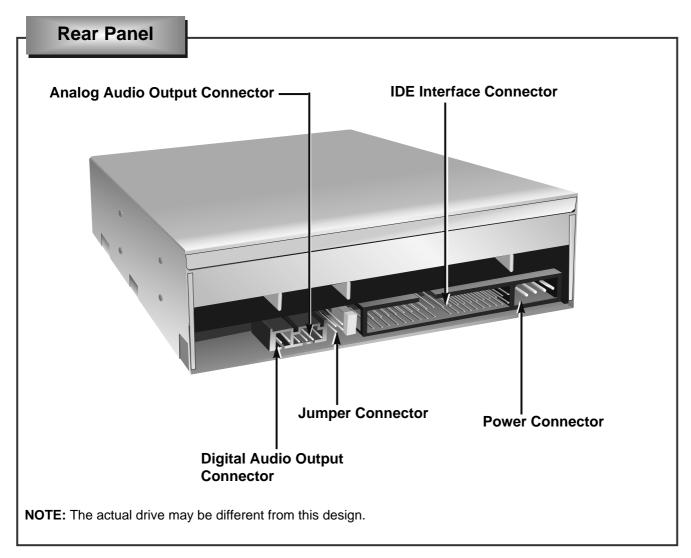
This button is pressed to open the CD tray. This button works only when power is supplied to the drive.

3. Emergency Eject Hole

Insert a paper clip here to eject the Disc tray manually or when there is no power.

4. Drive activity indicator

Two colored LED is used to indicate the operation of the Drive.



1. Power Connector

Connects to the power supply (5-and 12-V DC) of the host computer.

NOTE: Be careful to connect with the proper polarity. Connecting the wrong way may damage the system (and is not guaranteed). Usually this connector can only be attached one-way.

2. IDE Interface Connector

Connect to the IDE (Integrated Device Electronics) Interface using a 40-pin flat IDE cable.

NOTE: Do not connect or disconnect the cable when the power is on, as this could cause a short circuit and damage the system. Always turn the power OFF when connecting or disconnecting the cable.

3. Jumper Connector

This jumper determines whether the drive is configured as a master or slave. Changing the master-slave configuration takes effect after power-on reset.

4. Analog Audio Output Connector

Provides output to a sound card (analog signal). Generally you need this to play a regular audio CD

5. Digital Audio Output Connector

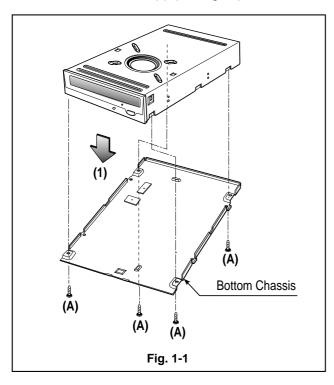
This connector is not supported.

DISASSEMBLY

1. CABINET and CIRCUIT BOARD DISASSEMBLY

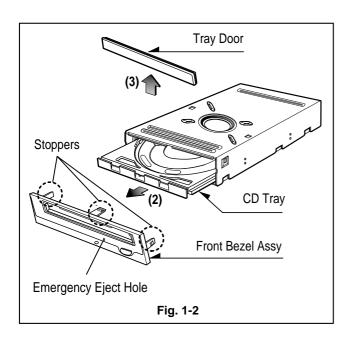
1-1. Bottom Chassis

A. Release 4 screws (A) and remove the Bottom Chassis in the direction of arrow (1). (See Fig.1-1)



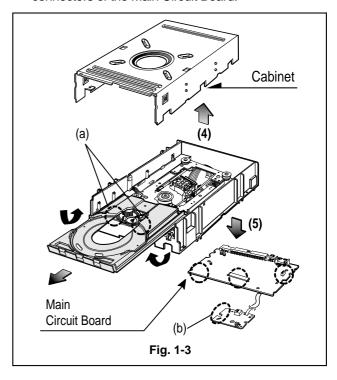
1-2. Front Bezel Assy

- A. Insert and press a rod in the Emergency Eject Hole and then the CD Tray will open in the direction of arrow (2).
- B. Remove the Tray Door in the direction of arrow(3) by pushing the stoppers forward.
- C. Release 3 stoppers and remove the Front Bezel Assy.



1-3. Cabinet and Main Circuit Board

- A. Remove the Cabinet in the direction of arrow (4). (See Fig. 1-3)
- B. When the CD tray has been opened completely, lift 2 points (a) and remove the CD tray while drawing out simultaneously.
- C. Remove the Soldering of the LD- and LD+ (b) for the Loading Motor, and then remove the Main Circuit Board.
- D. At this time, be careful not to damage the 4 connectors of the Main Circuit Board.

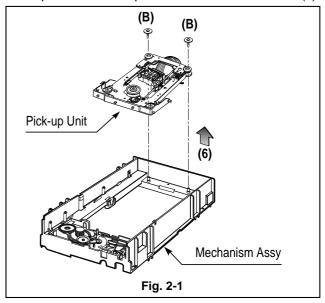


2. MECHANISM ASSY DISASSEMBLY

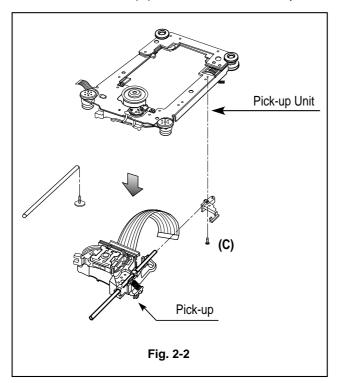
2-1. Pick-up Unit

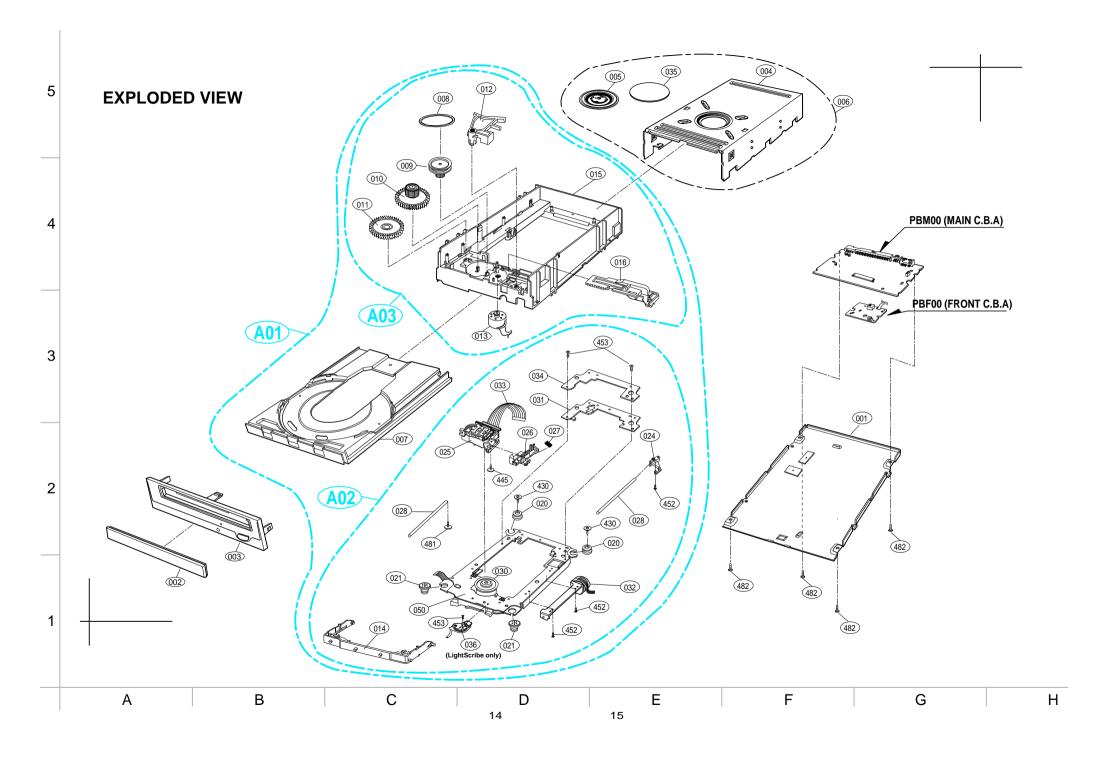
A. Release screws (B).

B. Separate the Pick-up Unit in the direction of arrow (6).



2-2. Pick-upA. Release 1 screw (C) and remove the Pick-up.





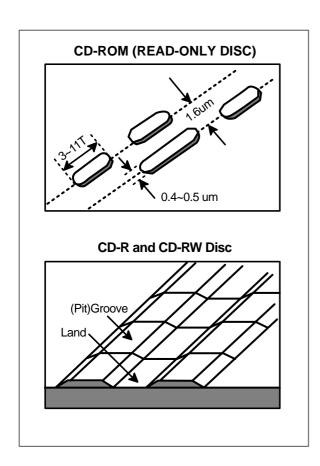
GLOSSARY

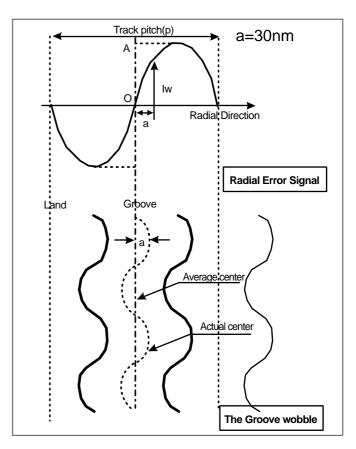
ATIP	Absolute Time in Pre-groove. With an additional modulation of the "Wobble", the "Groove" contains a time code information.				
Wobble	The pre-groove in the Disc is not a perfect spiral but is wobbled. With : – A typical amplitude of 30 nm – A spatial peried of 54~64 µm				
CW	Continuous Wave. The laser light output is at a constant level.				
DOW	Direct Over-Write. The action in which new information is recored over previously recorded information in CD-RW disc.				
Overwrite	The action in which new information is recorded over previously recorded information.				
(Pre-)Groove	The guidance track in which clocking and time code information is stored by means of an FM modulated wobble.				
Land	Land is characterized in the following way: When radial signals are concerned, land is defined as the area between the grooves. When HF signal are concerned, land is defined as the area between the marks(pits) in tangential direction.				
Hybrid Disc	A Multisession disc of which the first Session is mastered. On a hybrid disc, recorded and mastered information may co-exist.				
Mastered Information	Information,stored as pits on the disc during the manufacturing process of the disc. (when making the master)				
OPC	Optimum Power Control. Procedure is determined optimum recording power according to CD-R/RW Media in recording start step.				
ROPC	Running OPC. The purpose is to continuously adjust the writing power to the optimum power that is required. When the optimum power may change because of changed conditions of disc and change in operating temperature.				
Jitter	The 16 value of the time variation between leading and trailing edges of a specific (I3 I11) pit or land as measured by Time Interval Analysis.				
Deviation	The difference between a fixed value of Pit length and Land length.				
TOC	Table Of Contents: in the Lead-in Area the subcode Q-channel contains information about the Tracks on the disc.				
Packet Writing	A method of writing data on a CD in small increments. Two kinds of packets can be written: Fixed-length and Variable-length.				
Write Strategy	The shape of the HF write signal used to modulate the power of the laser. The Write Strategy must be used for recordings necessary for disc measurements.				
Information Area	Wobble, ATIP, Disc Identification, Write Power, Speed Range OPC Parameters, etc are recorded in the Information area of CD-RW Disc				
Finalization	The action in which (partially) unrecorded or logically erased tracks are finished and the Lead-in and/or Lead-out areas are recorded or overwritten with the appropriate TOC subcode.				
Logical Erase	A method to remove information from a disc area by overwriting it with an EFM signal containing mode 0 subcode A logically erased area is equivalent to an unrecorded				
Physical Erase	The action in which previously recorded information is erased by overwriting with a CW laser output. After a Physical Erase action, the erased area on the CD-RW disc is in the unrecorded state again.				
Session	An area on the disc consisting of a Lead-in area, a Program area, a lead-out area.				
Multi session	A session that contains or can contain more than one session composed Lead-in and Lead-out				

The differences of CD-R/CD-RW discs and General CD-ROM

1. Recording Layer

Recordable CD has a wobbled pre-groove on the surface of disc for laser beam to follow track.





2. Disc Specification

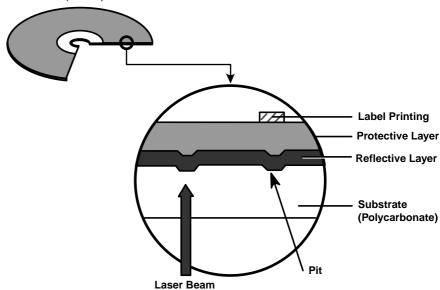
ITEM	CD-ROM	CD-R	CD-RW	
Standard	Yellow Book	Orange Book II	Orange Book III	
Record	Not available	Write once	Re-Writeable	
Tracking Signal I11/Itop (HF Modulation)	> 0.6	> 0.6	0.55 > M ₁₁ > 0.70	
Read Laser Power(mW)	< 0.5 mW	< 0.7 mW	< 1.0 mW	
Jitter	< 35 nsec	< 35 nsec	< 35 nsec	
Reflectivity (Rtop)	70 %	65 %	15 % ~ 25 %	
Remark) Write Laser Power(mW)		14-65 mW	6-45 mW	

3. Disc Materials

1) CD-ROM disc

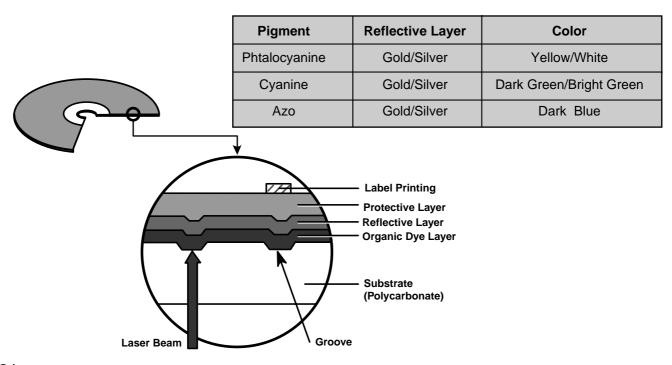
- It is composed of Silver _ colored aluminum plate and Reflective layer.
- Groove (Pit) of aluminum plate make a track.
- Laser wavelength: 780 nm, Laser Power (Read): 0.5mW

 Signal is detected by the difference of reflective beam intensity between "pit" and "Land" on the disc.

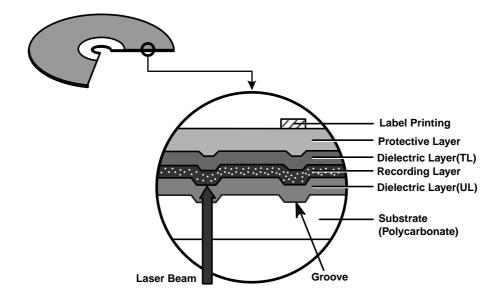


2) CD-R disc

- It is so-called WORM (Write Once Read Many) CD.
- It is composed of polycarbonate layer, Organic dye layer, Reflective layer, and Protective layer.Gold/Silver Reflective layer is used to enhance the reflectivity
- According to the kinds of Organic dye layer, it is divided by Green CD, Gold CD, Blue CD.
- Laser Wavelength: 780 nm, Laser Power (read): 0.7 mW
- Recording Power : 8x(14~20mW), 16x(25~35mW)
- When some part of dye layer is exposed to laser heat, it's color changs black. Therefore, writing and reading is enabled by the difference of reflectivity between changed part and unchanged part.
- Polycarbonate layer has Pre_Groove which make a Track.

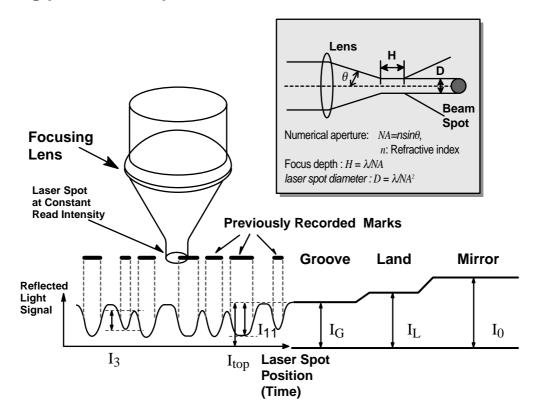


3) CD-RW Disc

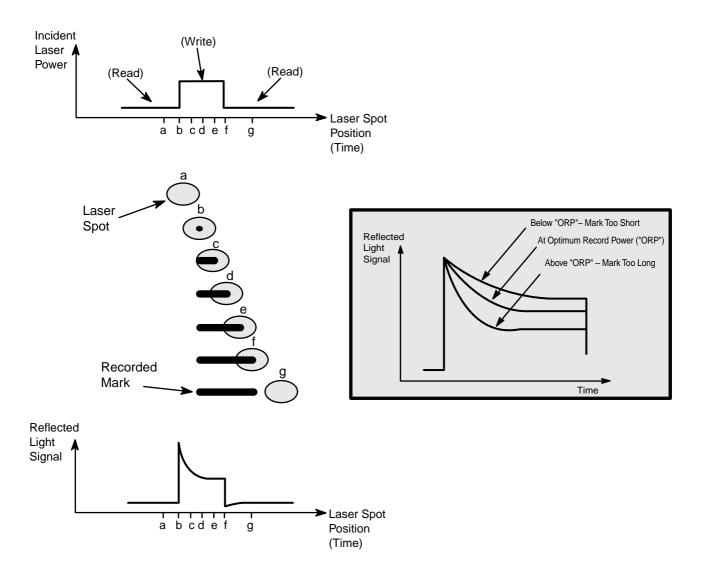


- It is composed of polycarbonate layer, alloy(silver, arsenic) layer, aluminum reflectivity layer, protective layer.
- An crystalized alloy layer is transformed into noncrystalized by the laser heat. Therefore, writing and reading is enabled by the difference of reflectivity.
- It is possible to overwrite about 1000 times.
- Laser Wavelength: 780 nm, Laser Power (Read): 1.0mW
- Recording Power : Erase (4~18mW), Write (6~45mW)
- When disc rewriting, new data is overwritten previously recorded data.
- Polycarbonate layer has a Pre-Groove which make a track.

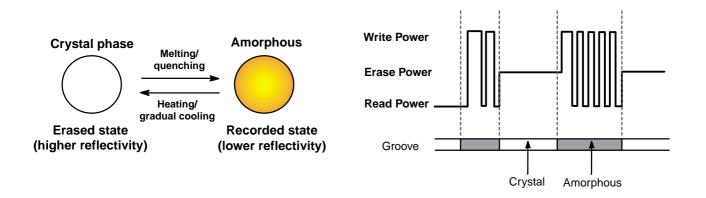
4. Reading process of Optical Disc



5. Writing Process of CD-R Disc

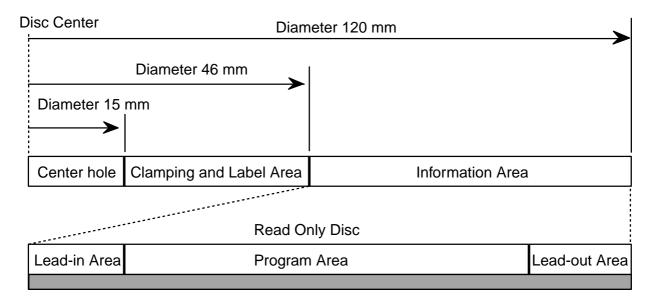


6. Writing process of CD-RW Disc

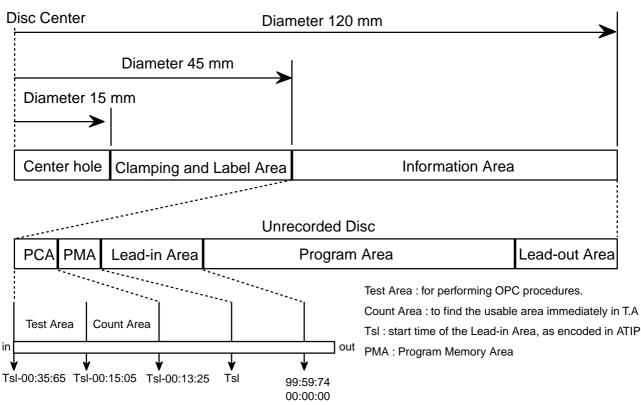


7. Organization of the PCA, PMA and Lead-in Area

1) Layout of CD-ROM disc



2) Layout of CD-R/RW disc



8. Function of PCA and PMA area

- 1) PCA (Power Calibration Area)
 - PCA area is used to determine the correct Laser Power for a disc.
 - Method 1 : PCA area is divided by a track.
 - Method 2: The previous Calibration value is referred.
 - Method 3: ROPC is used to determine Laser Power value automatically in data writing.
 - CD-R Disc can write maximum 99 Tracks but CD-RW Disc can write unlimited tracks because it has a rewritable function.

2) PMA (Program Memory Area)

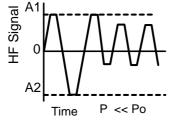
- It has a track information (track No, track Start/End time) of every track before writing completed.
 - PMA area has the last written point and the next writable point of a disc.
 - In case of CD to CD copy, some writer may not write PMA area.
- * When Disc is Finalized,

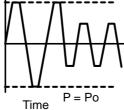
PMA information is transferred to the Lead_In area so that general Driver can read it.

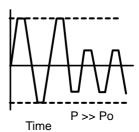
* Because PCA and PMA area exist before Lead-In area, General CD Player or CD-ROM Drive can't read these areas.

9. OPC and ROPC

- 1) OPC (Optimum Power Control)
 - This is the first step of writing process, because CD writer has its own laser power value and media have different writing characteristics,
 - This is determined by the Writing characteristic, speed, temperature, and humidity.
 - Laser wavelength is determined by the environmental temperature (775~795nm) and Optical Laser Power is determined by the test and retry.
 - Asymmetry and optimum writing Power
 - EFM signal Asymmetry is determined by the writing power.
 Therefore, Optical Power which has the same value to the preset power value can be estimated by measuring HF signal Asymmetry on the PCA area.
 - Measurement of Asymmetry
 - * Parameter setting (Beta) : Using AC coupled HF signal before equalization Beta = (A1+A2)/(A1-A2)

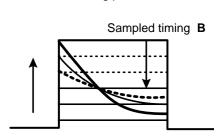






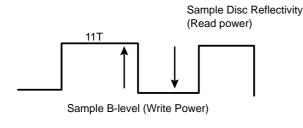
2) ROPC (Running Optimum Power Control)

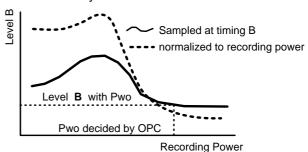
- Variable primary factor of Optimum Power
 - Change of Power sensitivity on the Disc. (limited to 0.05 *Po)
 - Wavelength shift of the laser diode due to the operating temperature change.
 - Change of the Spot aberration due to the Disc skew, Substrate thickness, Defocus.
 - Change of Disc or Optics conditions due to the long term OPC
 It is necessary to adjust continuously to obtain the Optimum Power.
- Principle of Running OPC
 - To meet the factors mentioned above,
 a horizontal _ direction movement of a curve is uesd.
 - Beta = f(B-level) = constant on the Recorded Disc
 - Procedure of ROPC
 - a. Reference B-level is determined during OPC Procedure.
 - b. During Recording, B-level value is controlled to have a close Reference B-level value.
 - c. Normalization of B-level is used to eliminate the effect of reflectivity fluctuation.
 - ==> The reflected B-level value is normalized by the disc reflectivity itself.



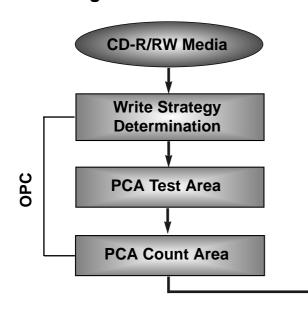
Reflected recording pulse

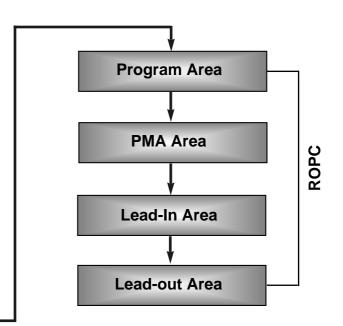
Incident recording pulse





10. Writing Process of DISC





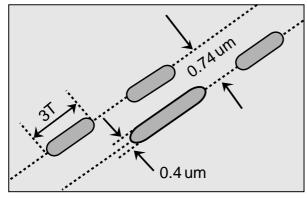
* Recording Capacity of CD-R/RW (74Minute Recording media)

- (2048 Byte/Sector) X (75 Sector/Second) X (60 Second/Minute) X 74 Minute
 = 681,984,000 Bytes = 682 Mbytes
- But the actual recording capacity is about 650 Mbytes. (according to the ISO 9660 standard, approximately 30 Mbytes are used to make directory structure and volume names.)

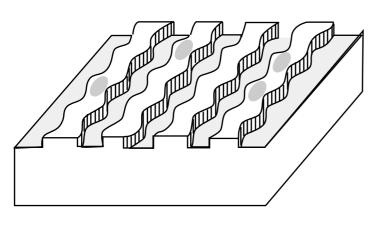
The differences of DVD-R/RW, DVD+R/RW discs and DVD-ROM

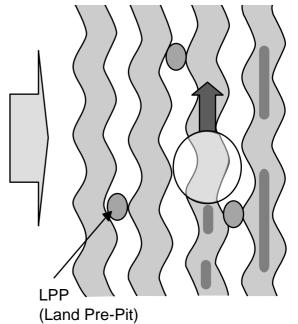
1. Recording Layer

DVD-ROM (Read Only Disc)

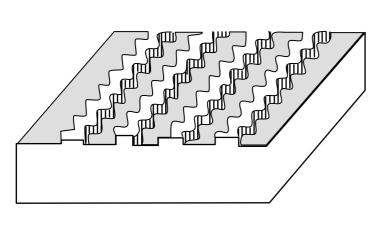


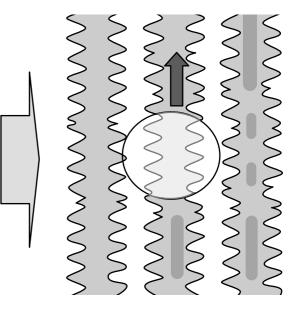
DVD-R/RW Disc





DVD+R/RW Disc



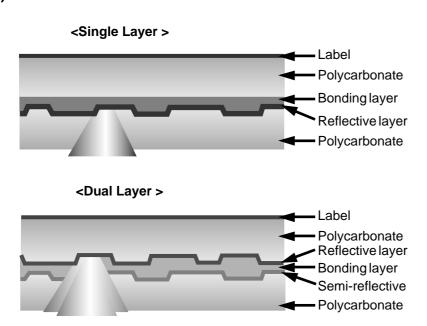


2. Disc Specification

	DVD-ROM		DVD-R	DVD-RW	DVD+R	DVD - DW
	Single-Layer	Dual-Layer	א-טעט-ג	DVD-RVV	DVD+R	DVD+RW
Media Type	Read Only	Read Only	Dye	Phase change	Dye	Phase change
User data capacity	4.7GB	8.54GB	4.7GB	4.7GB	4.7GB	4.7GB
Wavelength	650nm	650nm	650nm	650nm	650nm	650nm
Reflectivity	45~85%	18~30nm	45~85%	18~30%	45~85%	18~30nm
Track pitch	0.74 μm	0.74 μm	0.74 μm	0.74 μm	0.74 μm	0.74 μm
Minimum pit length	0.4 μm	0.44 μm	0.4 μm	0.4 μm	0.4 μm	0.4 μm
Modulation	>0.6	>0.6	>0.6	>0.6	>0.6	>0.6
Channel bit-rate	26.16MHz	26.16MHz	26.16MHz	26.16MHz	26.16MHz	26.16MHz
Wobble Frequency	-	-	140KHz	140KHz	817.4KHz	817.4KHz
Addressing	26.16MHz	26.16MHz	Wobble & LPP	Wobble & LPP	Wobble(ADIP)	Wobble(ADIP)
Read Power (mW)					0.7 ± 0.1	0.7 ± 0.1
Write Power (mW)	-	-				
Jitter	<8%	<8%	<8%	<8%	<9%	<9%

3. Disc Materials

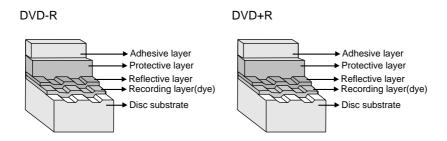
1) DVD-ROM



2) Recording format using organic dye material (DVD-R/DVD+R)

* The format that records data through the creation of recorded marks by changing the organic dye material with a laser beam.

> Disc structure



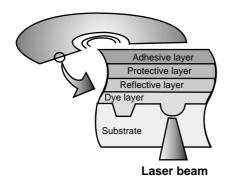
> Disc structure

[Recording]

Recording is done by changing the organic dye layer and the substrate with a laser when a strong is applied to a disc, the temperature of the ortanic dye material goes up, the dye is decomposed and the substrate changes at the same time. At this time, a durable bit is created as is the case with a CD-ROM.

[Playback]

Signals are read with the differences of the reflection of a laser from pits.

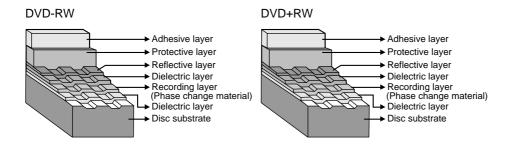


3) Recording format using phase-change recording material (DVD-RW/DVD+RW)

* Data is recorded by changing the recording layer from the amorphous status to the crystalline status, and played back by reading the difference of the reflection coefficient.

[Amorphous : Non-crystalline]

> Disc structure



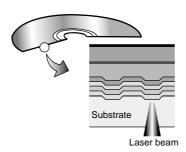
> Recording principles

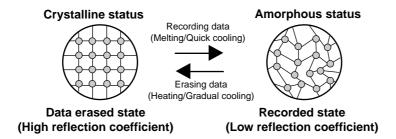
[Recording]

When a high-power laser is applied to the recording material, it melts and then becomes amorphous with a low reflection coefficient when it quickly cools off. When a mid-power laser is applied to heat gradually the recording material and then gradually cools it off, it becomes crystal with a high reflection coefficient.

[Playback]

A low-power laser is used for playback. The amount of reflected light depends on the status (amorphous or crystalline) of the recording material. This is detected by an optical sensor.





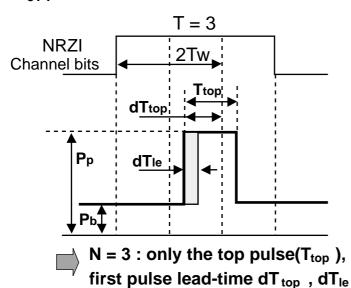
4. Writing Pulse Wave Form of DVD+R

For different speed ranges, different write strategies can be used. This document specifies 2 options:

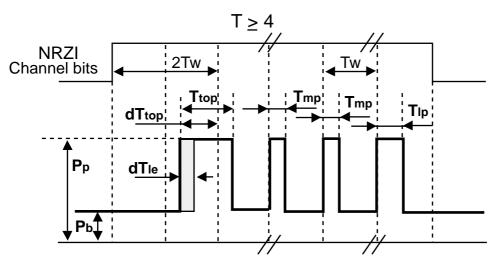
- a pulsed write strategy, where each single mark is created by a number of subsequent separated short pulses.
- a blocked write strategy, where each single mark is created by one continuous pulse.

1) 1st Method: Using Pulsed Write Strategy

* 3T :



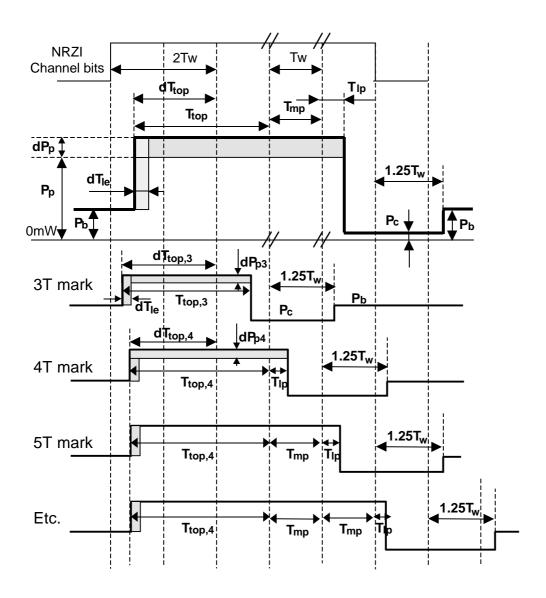
* ≥ 4T :



 $N \ge 4$: the top pulse (T_{top}), multi-pulse (T_{mp}) and last pulse (T_{lp}), first pulse lead-time dT_{top} , dT_{le}

Pp : Actual write power Pb : Bias Power

2) 2st Method: Using Blocked Write Strategy



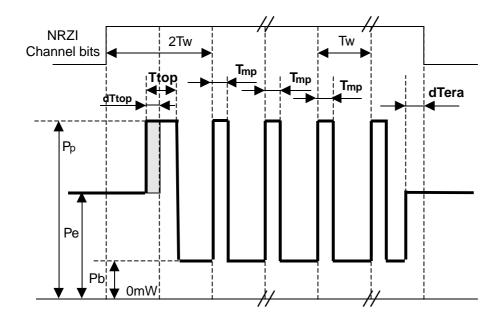
Pp: Actual write power

Pb: Bias Power

dPp : Additional power (Only be applied for the 3T and 4T marks)

Pc : Cooling power (Especially at higher recording speeds, optimum cooling down of the recording layer after writing a mark may be needed.)

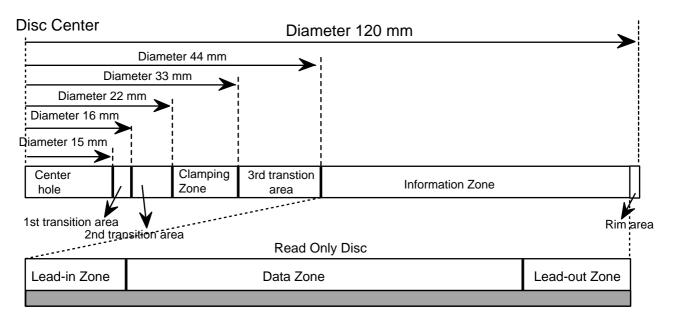
5. Writing Pulse Wave Form of DVD+RW



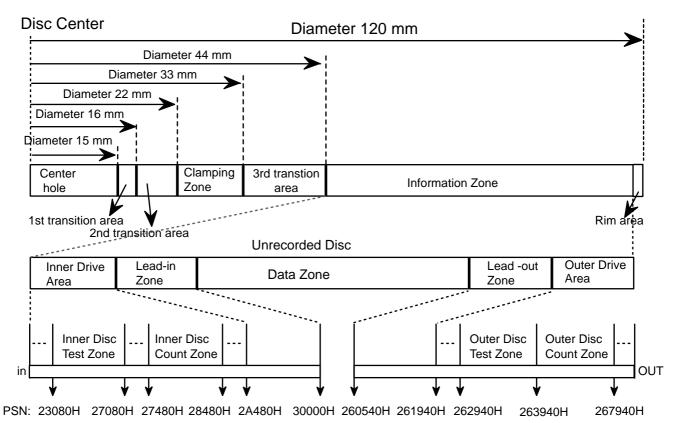
Pp : Actual write power Pe : Erase Power Pb : Bias Power

6. Organization of the Inner Drive Area, Outer Drive Area, Lead-in Zone and Lead-out Zone

1) Layout of DVD-ROM disc

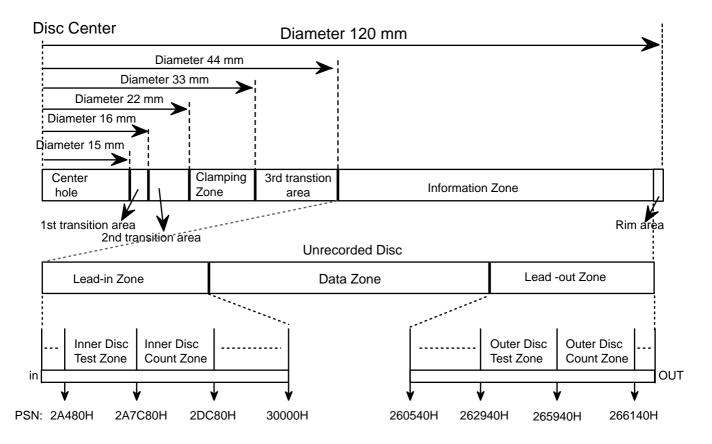


2) Layout of DVD+R disc



- > Inner Disc Test Zone : for performing OPC procedures.
- > Inner Disc Count Zone : for counting the number of OPC algorithm performed in IDT Zone.
- > Outer Disc Test Zone : for performing OPC procedures.
- > Outer Disc Count Zone : for counting the mumger of OPC algorithm performed in IDT Zone.

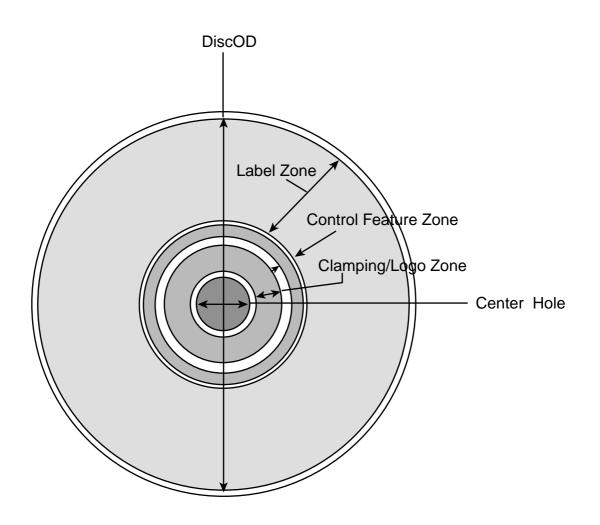
3) Layout of DVD+RW disc

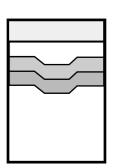


- > Inner Disc Test Zone : for performing OPC procedures.
- > Inner Disc Count Zone : for counting the number of OPC algorithm performed in IDT Zone.
- > Outer Disc Test Zone : for performing OPC procedures.
- > Outer Disc Count Zone : for counting the number of OPC algorithm performed in IDT Zone.

LightScribe Media

1. LightScribe Media

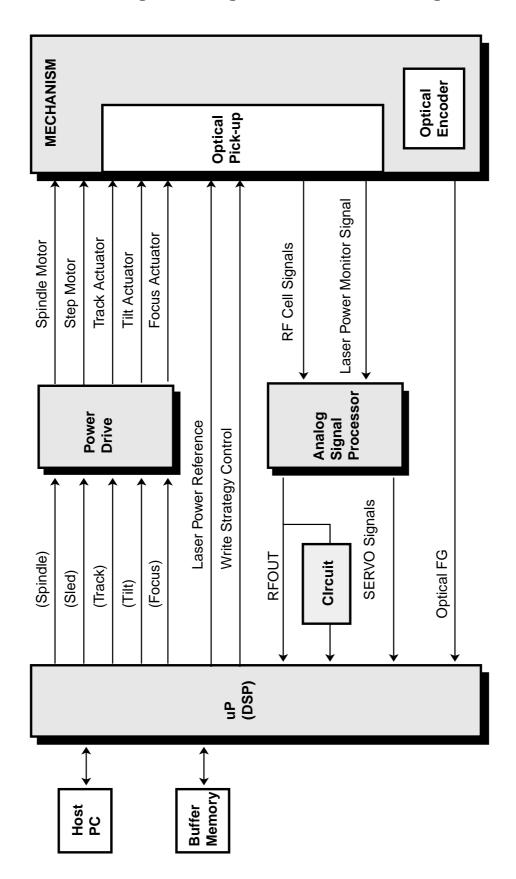




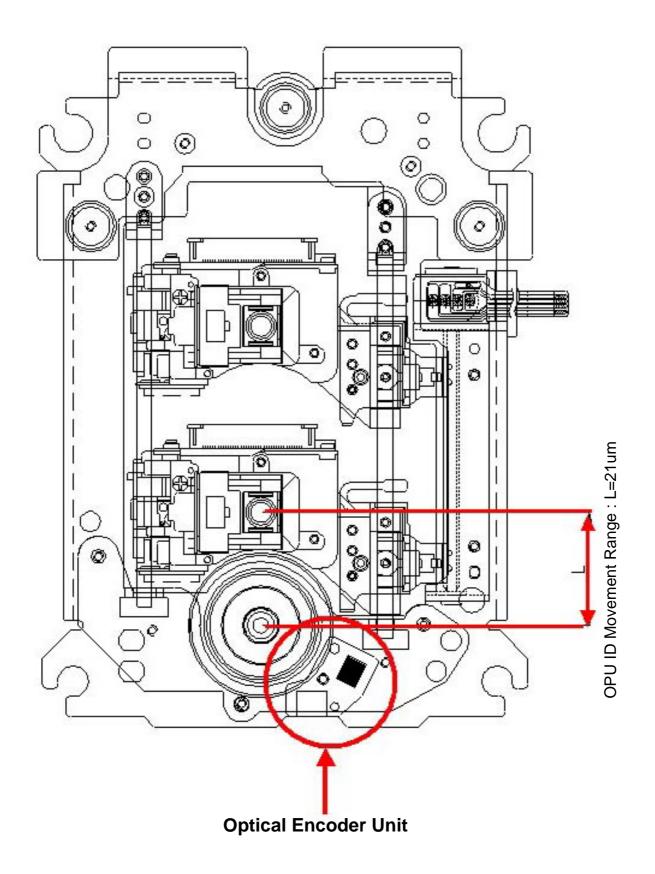
Screen Printed Imaging Layer Clear Protective Coating Reflective/Thermal Layer Dye Data Layer

Polycarbonate Substrate

2. Hardware Block Diagram of LightScribe Label Printing

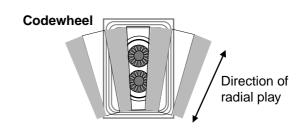


3. MD Assy For LightScribe



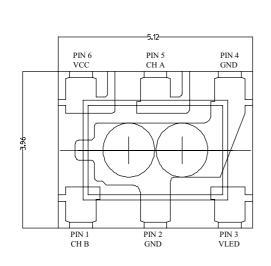
4. Optical Encoder Assy

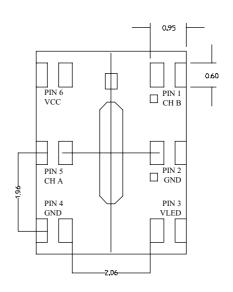




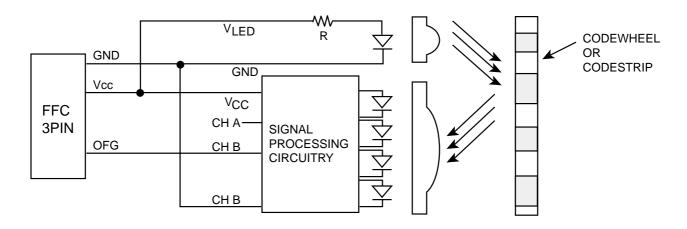
Encoder PCB

Optical Encoder IC



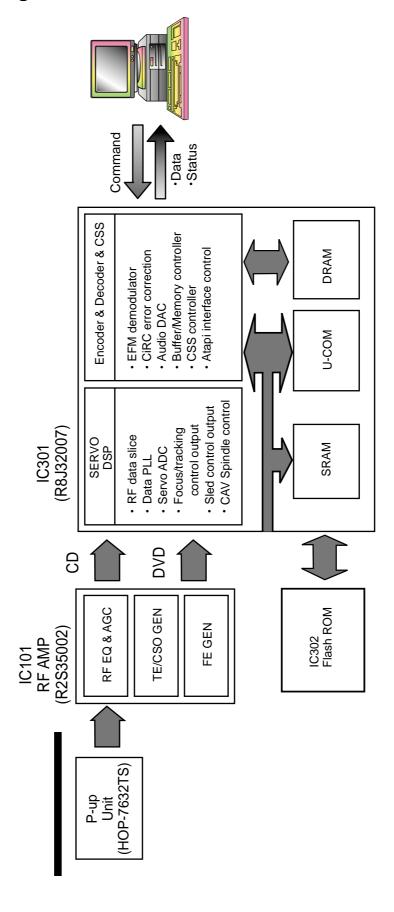


Schematic of Enc PCB



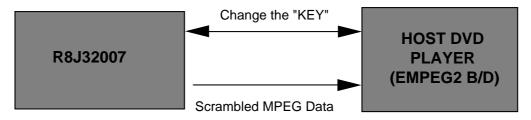
DVD & CD DATA PROCESSING

1. Data Processing Flow



2. Copy Protection and Regional Code Management Block

Block Diagram



KEY Management Control

Brief Process

1. Regional Code for DVD Disc

DVD-ROM drive transfers the regional code of the control data to host by the command of host, the DVD player of host reads the regional code, and plays title in the case of allowed regional code only.

2. Management of DVD Disc for the scrambled of data

- (1) DVD-ROM and DVD player of host generate the "KEY 1" respectively, transfer to opposite part, the "KEY 2" is received, recognizes the data transfer or not with this value, and generates the bus key encoded the data.
- (2) Encoded "Disc Key" and "Title Key" host is transfer with the bus Key.
- (3) DVD player of host reads the key value, and uses the value to restore the scrambled data.
- * Refer to the next page for the details.

3. About Prevention the DVD-ROM from to be copy

A data is able to encode and record in the disc, if a copyright holder wants to prevent the disc from copying.



In case of a disc enhanced movie of 3 titles......

DISC KEY (2048 Bytes) is used to encode the whole contents in the disc and TITLE KEY (5 Bytes) is used to encode the title respectively.

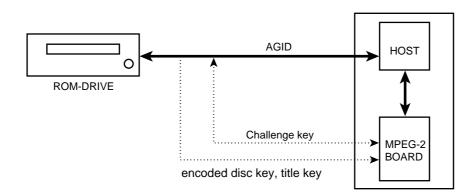
So, the data is encoded and stored in a disc through the unknown algorithms with a disc key and title key. (At this time, the disc key and title key are stored in a disc.)

...As above, the disc is able to copy when the disc key and title key are opened.

Then, ROM-DRIVE encodes the disc key and title key and transfers to MPEG-2 board.

If you want to play the disc prevented from the copy......

First of all, ROM-DRIVE and MPEG-2 board identify with each other through the procedure as described below.



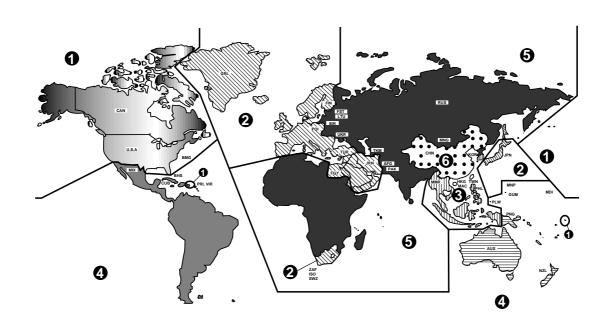
- 1. Drive and host gives and takes the ID of 2bit. This ID is AGID (Authentication Grant ID).

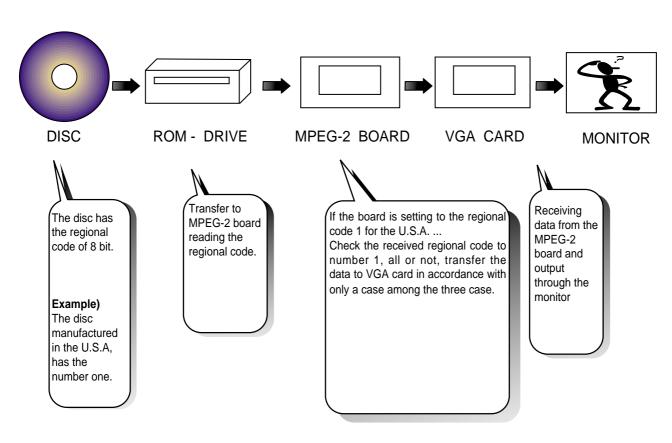
 The various decoder boards are attached to the host, in these, AGID sets the MPEG-2 board and drive.
- 2. After the AGID is set, MPEG-2 board generates the challenge key (10 Byte) and transfers to drive. The board and drive generate key 1 (5Byte) with the challenge key respectively. (Of course, the Algorithm generating the key 1 is not known.)
- 3. Compare with the generated key 1, if it corresponds each other, the first step of authentication is completed. This is a course to identify the MPEG-2 board with a drive.
- 4. The second step of authentication is a course to identify a drive with the MPEG-2 board.

 The dirve generates a challenge key and transfers it to the MPEG-2 board. The dirve and MPEG-2 board generate the key 2 (5Byte) with the challenge key, compare with each other, and if it corresponds and the secondary step of authentication is completed.
- 5. As above, the identification is completed.
- 6. The dirve and MPEG-2 board generate the Bus key with the key 1 and key 2 and own it.
- 7. Dirve encodes the disc key and title key with this Bus key and transfers to the MPEG-2 board.
- 8. The MPEG-2 board reads the encoded disc key and title key with the Bus key only.
- 9. MPEG-2 board lets data read from the drive to decode with the read disc key and title key and makes into the video signal by decoding.

4. About the DVD-ROM Regional Code

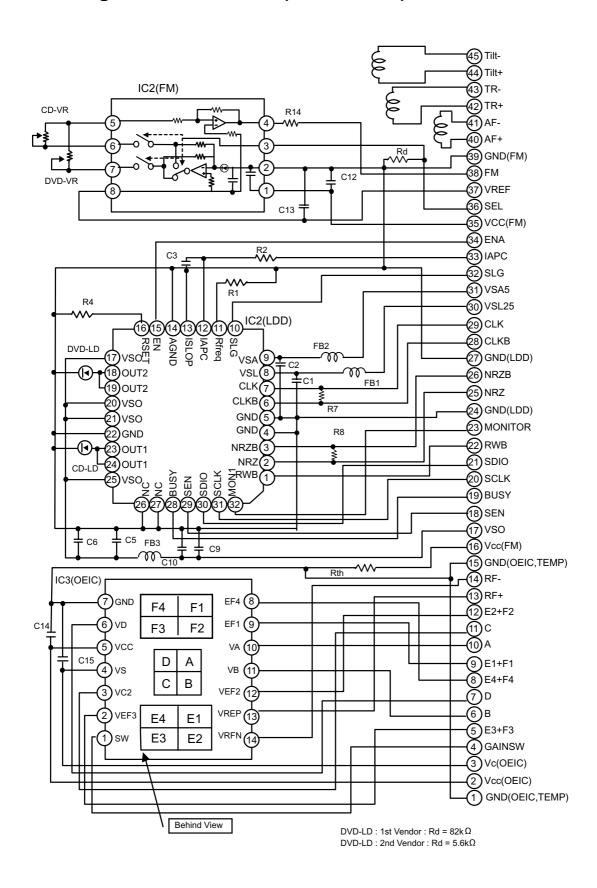
Regional code





INTERNAL STRUCTURE OF THE PICK-UP

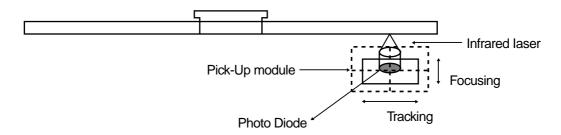
1. Block Diagram of the PICK-UP(HOP-7632TS)



2. Pick up Pin Assignment

No.	Signal Name	I/O	Signal Description			
1	GND(OEIC,TEMP)		Ground for OEIC			
2	Vcc(OEIC)	I	Power supply for OEIC			
3	Vc(OEIC)	I	Reference voltage input for OEIC			
4	GAINSW	I	OEIC output gain control (High:Low gain, Middle:Middle gain, Low:High gain)			
5	E3+F3	0	Single OEIC output EF3			
6	В	0	Single OEIC output B			
7	D	0	Single OEIC output D			
8	E4+F4	0	Single OEIC output EF4			
9	E1+F1	0	Single OEIC output EF1			
10	Α	0	Single OEIC output A			
11	С	0	Single OEIC output C			
12	E2+F2	0	Single OEIC output EF2			
13	RF+	0	Single OEIC RF positive differential output			
14	RF-	0	Single OEIC RF negative differential output			
15	GND(OEIC.TEMP)	0	Ground for OEIC and TEMP			
16	TEMP	0	Output voltage for controlling temperature			
17	VSO	I	Supply voltage for the output drivers only			
18	SEN	I	Serial control enable (H=enable, L=disable)			
19	BUSY	0	Goes high when serial transfer to timing menory is active			
20	SCLK	I	Serial control clock			
21	SDIO	I/O	Serial data for parameters and control ; in/out			
22	RWB	I	Write enable for NRZ laser data (L=write, H=read)			
23	MONITOR	0	Monitor output			
24	GND(LDD)		Ground connection for LD Driver-IC			
25	NRZ	I	NRZ laser data (H=mark, L=space) (LVDS+)			
26	NRZB	ı	NRZ laser data (H=mark, L=space) (LVDS-)			
27	GND(LDD)		Ground connection for LD Driver-IC			
28	CLKB	Ι	CLOCK for NRZ code input (LVDS-)			
29	CLK	Ι	CLOCK for NRZ code input(LVDS+)			
30	VSL25	_	Supply voltage for 2.5V logic			
31	VSA5	Ι	Supply voltage for PLL only			
32	SLG	Ι	Land/groove input serects the power register set (H=land, L=groove)			
33	IAPC	Ι	A low inpedance current input; 100xIAPC frow to the output			
34	ENA	I	Fast chip enable input			
35	VCC(FM)	I	Power supply for FM			
36	SEL	I	Low: selects DVDFMOUT			
			High: selects CDFMOUT			
37	VREF	I	APC amplifier reference voltage input			
38	FM	0	APC amplifier output			
39	GND(FM)		Ground connection for FM			
40	AF+	I	Focusing Actuator drive signal+			
41	AF-	I	Focusing Actuator drive signal-			
42	TR+	I	Tracking Actuator drive signal+			
43	TR-	I	Tracking Actuator drive signal-			
44	Tilt+	I	Tilting Actuator drive signal+			
45	Tilt-	I	Tilting Actuator drive signal-			

3. Signal detection of the P/U



1) Focus Error Signal ==> (A+C)-(B+D)

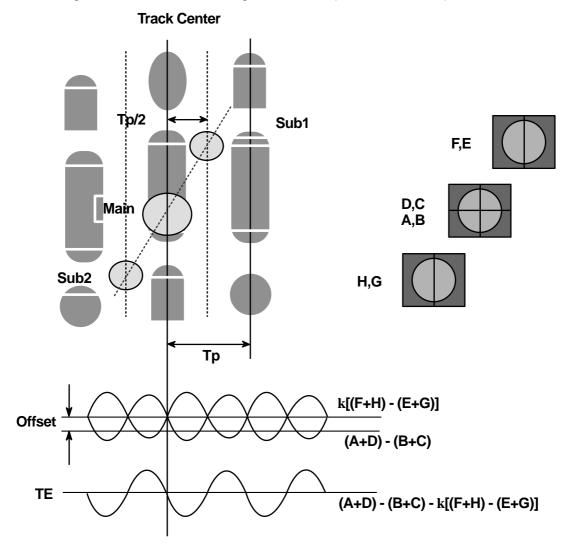
This signal is generated in RF IC (IC101 : R2S35002) and controls the pick-up's up and down to focus on Disc.

2) Tracking Error Signal (DPP Method) ==> $\{(A+D)-(B+C)\}-k \times \{(EF_1+EF_4)-(EF_2+EF_3)\}$

This signal is generated in RF IC (IC101: R2S35002) and controls the pick-up's left and right shift to find to track on Disc.

3) RF Signal ==> (A+B+C+D)

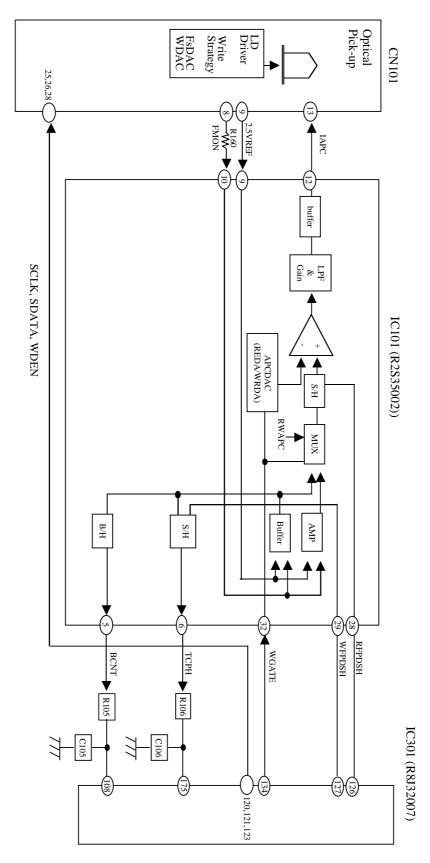
This signal is converted to DATA signal in DSP IC (IC301: R8J32007).



DESCRIPTION OF CIRCUIT

1. ALPC (Automatic Laser Power Control) Circuit

1-1. Block Diagram



1-2. ALPC (Automatic Laser Power Control) Circuit

ALPC function DVD/CD anlang front-end IC(IC101 R2S35002) is for constant power control purpose. Based on the accurate power sensor(FMON) in P/U, ALPC feedback loop maintains constant power level against laser diode's temperature variation.

The ALPC loop amplifies(10x) the FMON signal to enhance the accuracy of read power level control. Swithching of amplification is made by combination of a logical WGATE signal and a logical RWAPC signal.

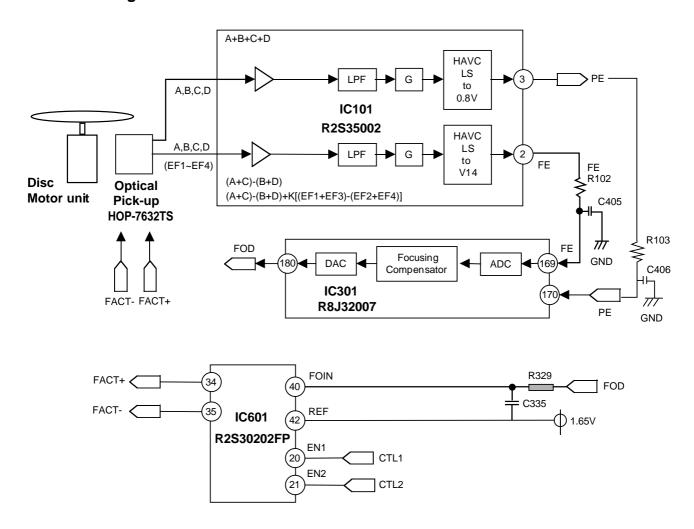
There are two set of APCDAC, which are used at different term to monitor different power level. Generally, the one is used at reading and the other one is used at writing. The logical WGATE signal which is switched between reading and writing changes the two APCDAC.

The ALPC loop supplies same currency (IAPC) to Laser Diode Driver(LDD) during reading and writing.

There is another ALPC which controls Full-Scale-DAC (FsDAC). FsDAC determines scale of WDAC of Laser Diode Driver. MPU monitors write-power level of FMON signal and changes FsDAC directly to maintain constant write-power level. There are two write power signal. The one is based on S/H signal and the other one is based on B/H(Bottom-Hold) signal. The write power levels are monitored as digital levels which are converted by built-in Anlog-Digital Converter in DSP. The MPU monitors each write power level and calculates proper setting of FsDAC, and changes value through serial interface between LDD and DSP.

2. Focus Circuit

2-1. Block Diagram



2-2. Focus Servo

The aim of Focus Servo is to maintain the distance between object lens of P/U and disc surface, so that the detected RF signal(A, B, C, D, EF1, EF2, EF3, EF4) can be maximized.

Focus Error Signal(FE) generates from focus error detection block in RF IC(R2S35002) using Conventional Astigmatism Detection method, Differential Astigmatism Detection method.

Focus Gain and path can be changed at the RF IC(R2S35002) according to the disc, and the resulting output FE(R2S35002 2pin) is input to DSP IC(R2S35002 169pin).

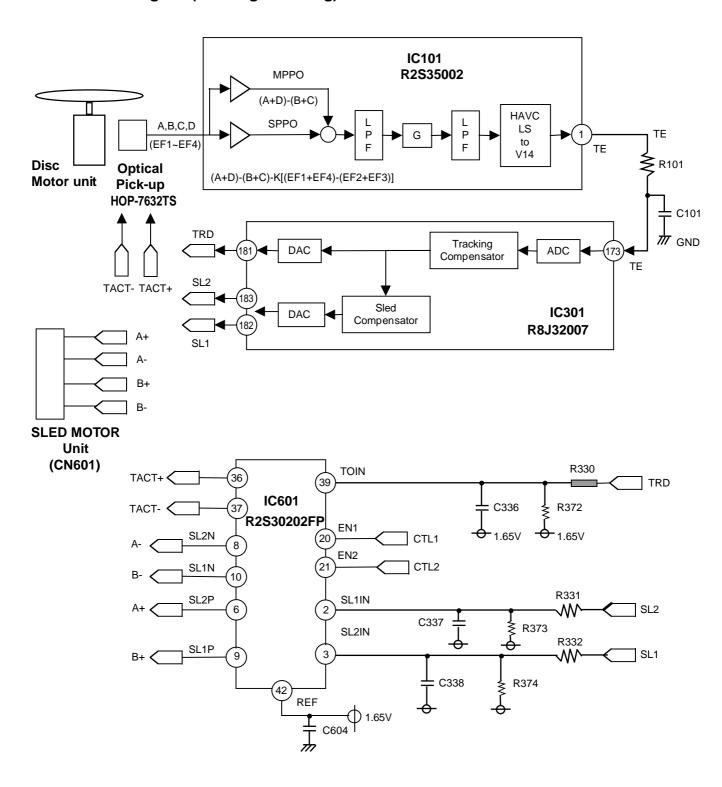
The Focus Search operation is using FE, PE Signal, therefore check FE, PE signals when Focusing is failed.

The role of DSP IC(R8J32007) is Focus Digital Controller. The operation path is as follows;

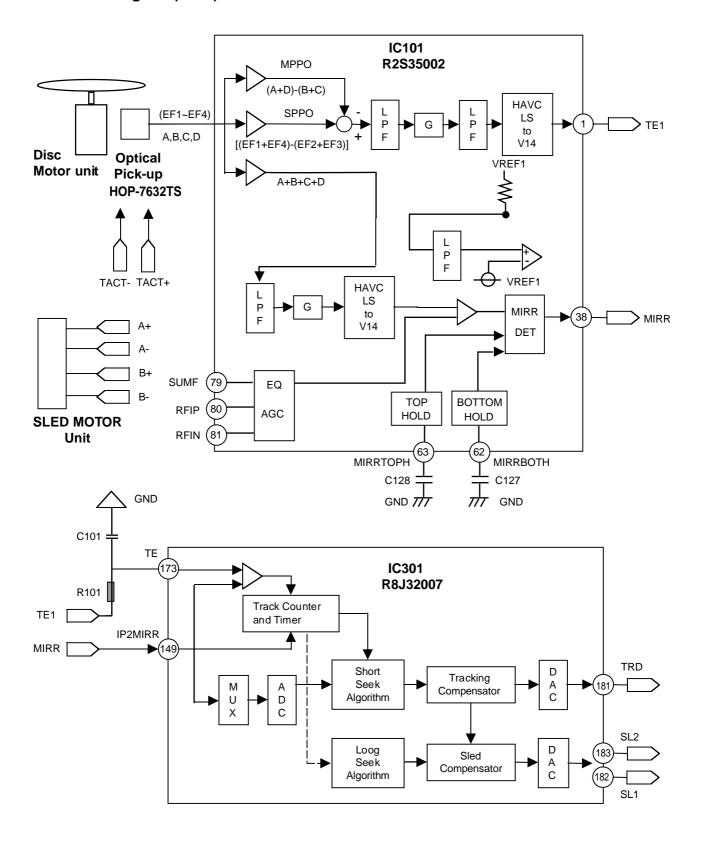
FE Signal is input to DSP IC(R8J32007 169pin), and after A/D Conversion, Digital Equalizer Block and D/A Conversion in R8J32006FP, the output signal FOD(R8J32007 180pin) is input to Drive IC(R2S30202FP 40pin). The drive output signal FACT+/FACT- generated according FOIN(R2S30202FP 40pin), and drives focus actuator in the P/U unit.

3. Tracking & Sled Circuit

3-1-1. Block Diagram (Tracking Following)



3-1-2. Block Diagram (Seek)



3-2-1. Tracking Servo

The aim of tracking servo is to make laser beam trace the data track on disc.

Tracking Error(TE) Signal is generated from tracking error detected block in R2S35002 using DPP(Differential Push-Pull) Method and DPD (Differential Phase Detection) Method.

DPP Method uses not only main beam(A, B, C, D) but also side beam(EF1~EF4) for correcting DC offset generated in Push-Pull Method.

The remaining procedure of TE signal processing in R8J32007 is similar to Focus Servo.

The role of DSP IC(R8J32007) is Tracking Digital Controller.

TE Signal is input to DSP IC(R8J32007 173pin), and after A/D Conversion, Digital Equalizer Block and D/A Conversion in R8J32007, the output signal TRD(R8J32007 181pin) is input to Drive IC(39pin).

The drive output signal TACT+/TACT- generated according TOIN(R2S30202FP 39pin), and drives tracking actuator in the P/U unit.

3-2-2. Sled Servo

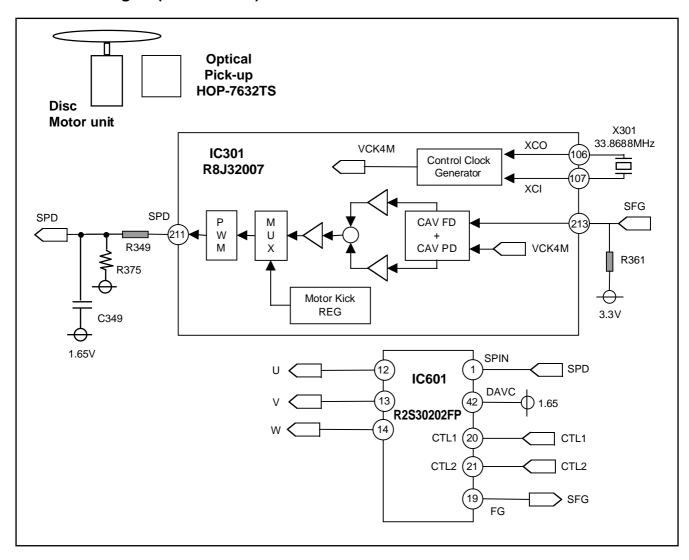
The working distance of tracking actuator is too short to cover whole disc radius.

Sled Servo make P/U move by little and little so that the laser beam keep tracing the data track on disc continuously when tracking actuator reaches the working limit.

TE Signal is input to DSP IC(R8J32007 173pin), and after A/D Conversion, Digital Tracking Equalizer Block, Digital Sled Compensator Block and D/A Conversion in R8J32007, the output signal SL1, SL2(R8J32007 182, 183pin) is input to Drive IC (R2S30202FP SL1:3 pin, SL2:2pin) after Low-Pass filtering.

4. Spindle Circuit

4-1-1. Block Diagram(FGCAV Servo)



4-1-2. FG CAV Servo

1) CD 48x CAV: CD-ROM, CD-R

2) CD 40x CAV : CD-RW
3) DVD 8x CAV : DVD±RW
4) DVD 10x CAV : DVD±R
5) DVD 12x CAV : DVD-ROM DL
6) DVD 16x CAV : DVD-ROM
7) DVD 16x PCAV : DVD±R

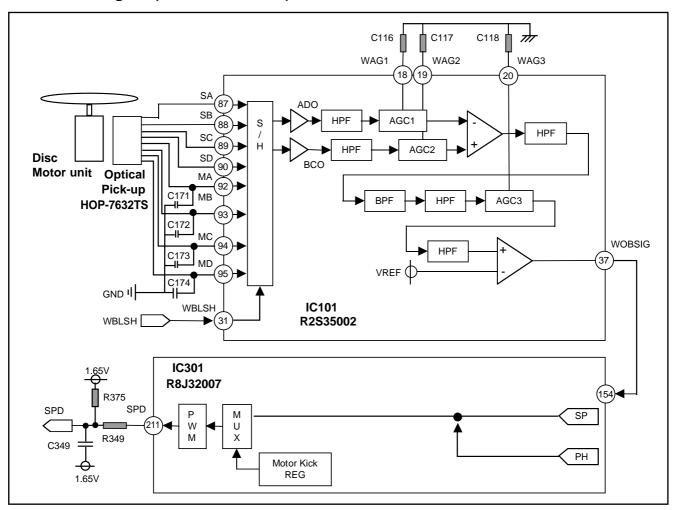
When drive read PRESS CD, Closed Session CD-R/RW, the spindle motor is controlled using FG CAV Spindle Servo. FG signal(R2S30202FP 19pin) input to SFG in DSP IC(R8J32007 213pin).

The spindle controller in DSP IC uses SFG as spindle rotation frequency feedback, therefore the FG CAV Spindle Servo doesn't work well if FG generation is abnormal.

The spindle controller PWM output signal SPD(R8J32007 211pin) input to SPIN in Drive IC(R2S30202FP 1pin) after Low-Pass Filtering.

The PWM output signal U, V, W signal(R2S30202FP 12, 13, 14pin) drives Spindle Motor without using a sensor, and FG pulse output is generated as 18 pulses/rotation.

4-2-1. Block Diagram (Wobble CLV Servo)



4-2-2. Wobble CLV Servo

CD-R: 4x, 8x, 16x, 24x, 32x, 40x, 48x

/CD-RW: 4x, 10x, 16x, 24x, 32x /DVD-R: 2x, 4x, 8x, 16x(PCAV)

/DVD-R DL : 2x, 4x

/DVD-RW : 1x, 2x, 4x, 6x

/DVD+R: 2.4x, 4x, 8x, 12x, 16x(PCAV)

/DVD+R DL : 2.4x, 4x, 6x

/DVD-RAM : 2x, 3x, 3-5x(PCAV)

/DVD+RW : 2.4x, 4x, 8x

When drive write DVD-RAM/R/RW/+R/+RW/CD-R/CD-RW, the spindle motor is controlled using Wobble CLV Spindle Servo.

The WOBSIG signal(R2S35002 37pin) input to DSP IC(R8J32007 154pin). The DSP Controller in R8J32007 uses WOBSIG as linear velocity feed back, therefore the Wobble CLV Spindle Servo doesn't work well when WOBSIG signal is abnormal.

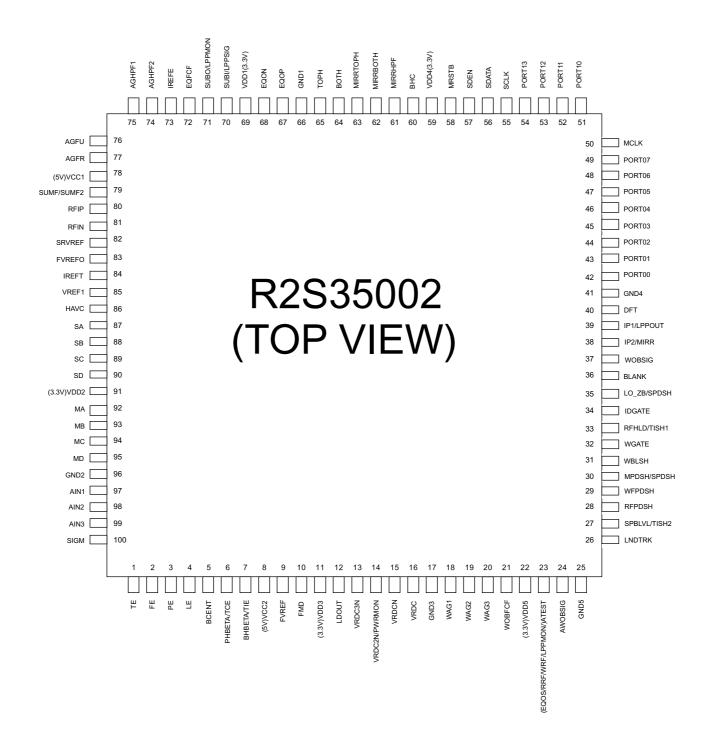
The spindle controller PWM output signal SPD (R8J32007 211pin) input to SPIN in Drive IC(R2S30202FP 1pin) after Low-Pass Filtering.

The PWM output signal U,V, W signal (R2S30202FP 12, 13, 14pin) drives Spindle Motor without using a sensor.

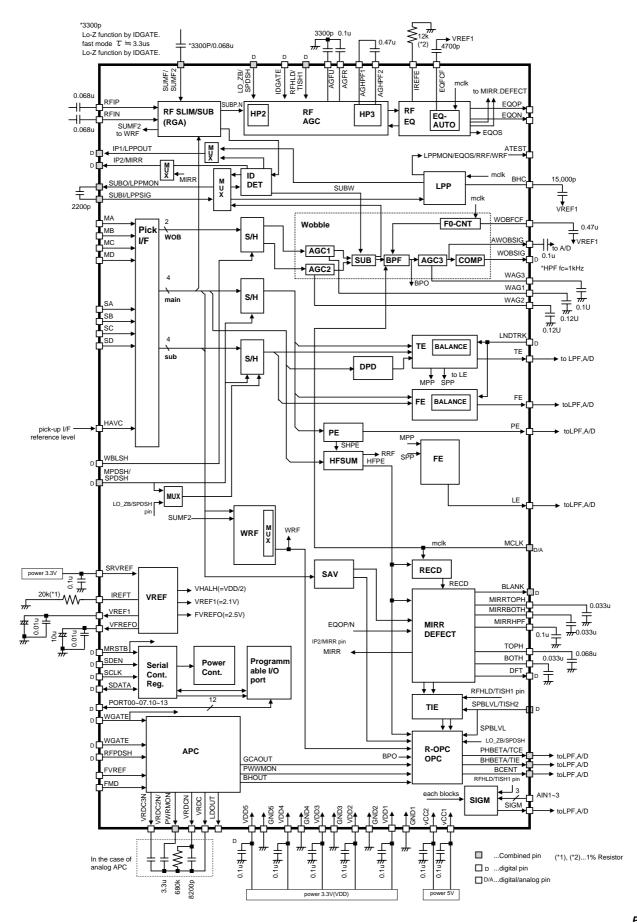
MAJOR IC INTERNAL BLOCK DIAGRAM AND PIN DESCRIPTION

IC101 (R2S35002): RF AMP Analog Signal Processor

Pin Assignment



Block Diagram



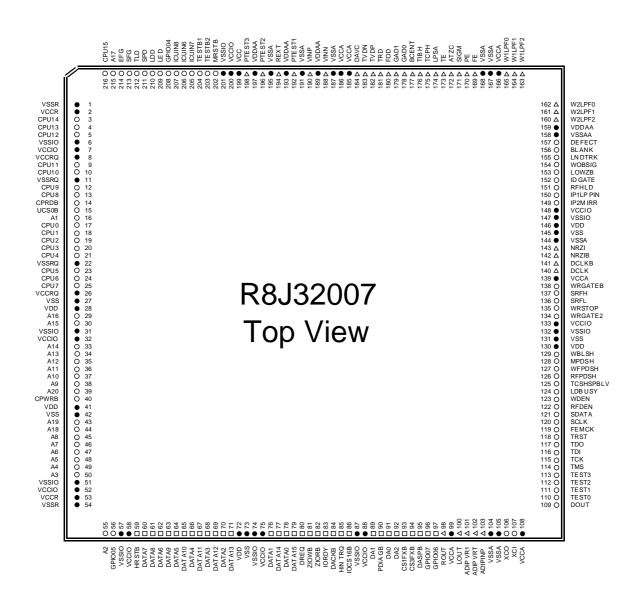
• Pin Functions

pin Name	pin No.	Туре	max. voltag	ge	Function
TE	1	Analog-Output			Tracking error output terminal
FE	2	Analog-Output			Focus error output terimnal
PE	3	Analog-Output			PE output terminal
LE	4	Analog-Output			Lens error output terminal
BCENT	5	Analog-Output			OPC center signal output terminal
PHBETA/TCE	6	Analog-Output			OPC top hold level signal and APC write sampleing
					signal output terminal/tilt servo detecting output terminal
BHBETA/TIE	7	Analog-Output			OPC bottom hold level signal and R-OPC sampleing
					signal output terminal/tilt servo detecting output terminal
VCC2	8	Power			Power supply connected terminal(5V)
FVREF	9	Analog-Input		VDD	Reference voltage for APC input terminal
FMD	10	Analog-Input		VDD	APC monitor diode input terminal
VDD3	11	Power			Power supply connected terminal(3.3V)
LDOUT	12	Analog-Output			Terminal to control laser drivers for APC read system
VRDC3N	13	External-compor	nents required		Terminal to connect laser driver control filters for APC
		·	•		read
VRDC2N/PWRMON	14	External-compor	nents required		Terminal to connect laser driver control filters for APC
		· · ·			read/ SH monitor output terminal
VRDCN	15	External-compor	nents required		Terminal to connect laser driver control filters for APC
					read
VRDC	16	External-compor	nents required		Terminal to connect laser driver control filters for APC
		·			read
GND3	17	Ground			Ground connected terminal
WAG1	18	External-capacito	or required		Terminal to connect WOBBLE AGC detector capacitor
WAG2	19	External-capacito	•		•
WAG3	20	External-capacito	•		
WOBFCF	21	External-capacitor required			WOB-BPF f0 auto-adjustment external capacitor
		·	·		connected terminal
VDD5	22	Power			Power supply connected terminal(3.3V)
ATEST	23	Analog-Output			Renesas analog test signal output terminal
AWOBSIG	24	Analog-Output			Analog-level WOBBLE signal output terminal
GND5	25	Ground			Ground connected terminal
LNDTRK	26	Digital-Inputpull-	JD QL	VDD	Balans adjustment mode selection
SPBLVL/TISH2	27	Digital-Inputpull-	•	VDD	R-OPC WRF signal sampling pulse input terminal
		0 1 1			/Tilt servo detecting sampling pulse input terminal
RFPDSH	28	Digital-Input	putpull-up	VDD	APC read system sampling pulse input terminal
WFPDSH	29	Digital-Input	putpull-up	VDD	APC write system sampling pulse input terminal
MPDSH/SPDSH	30	Digital-Input	putpull-up	VDD	Pickup input sampling pulse input terminal
WBLSH	31	Digital-Input	putpull-up	VDD	WOBBLE sampling pulse input terminal
WGATE	32	Digital-Input	putpull-up	VDD	Read/write control input terminal
RFHLD/TISH1	33	Digital-Input	putpull-up	VDD	RF hold control signal input terminal /Tilt servo detecting
		3	L. dram alk		sampling pulse input terminal
IDGATE	34	Digital-Input	putpull-up	VDD	ID select pulse input terminal
LO_ZB/SPDSH	35	Digital-Input	putpull-up	VDD	Low-z (reversal) pulse input terminal
	00	Digital hiput	Parbaii ap	, 55	/Pickup input sampling pulse input terminal

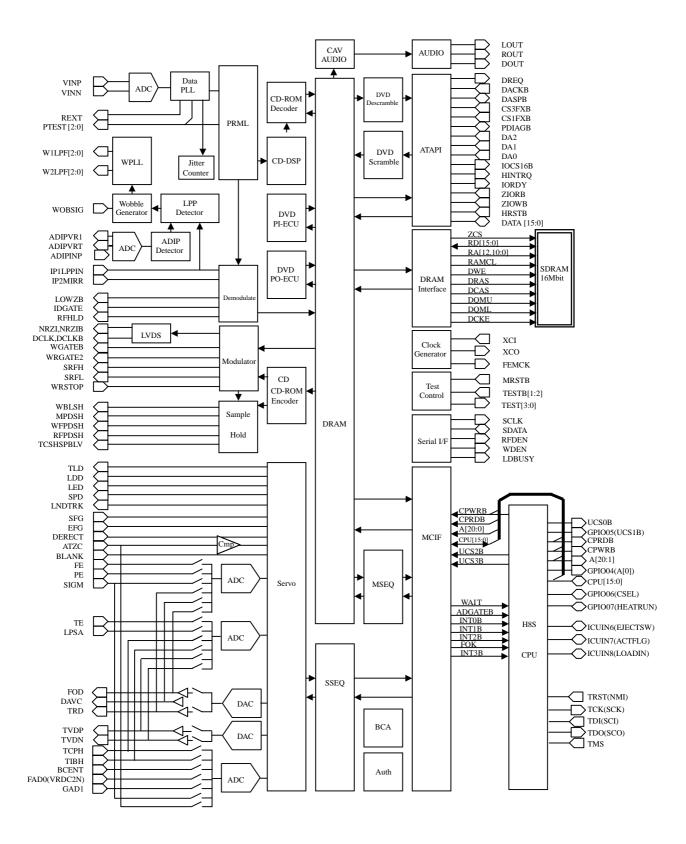
pin Name	pin No.	Туре	max. volta	age	Function
BLANK	36	Digital-Output			Record/non-record detecting/BD detecting output
					terminal
WOBSIG	37	Digital-Output			WOBBLE signal output terminal
IP2/MIRR	38	Digital-Output			ID detection/Mirror detection output terminal
IP1/LPPOUT	39	Digital-Output			ID detection/LPP detection output terminal
DFT	40	Digital-Output			Defect detection output terminal
GND4	41	Ground			Ground connected terminal (Digital)
PORT00	42	Digital-Input/Output		VDD	I/O Port
PORT01	43	default input mo	de		
PORT02	44	No	pull-up		
PORT03	45				
PORT04	46				
PORT05	47				
PORT06	48				
PORT07	49				
MCLK	50	Digital/Analog-Input		VDD	Main clock input terminal
		No	pull-up		Equalizer fc auto-adjustment control clock input terminal.
					LPP output pulse width control clock input terminal.
					WOB-BPF f0 auto-tracking clock input terminal.
PORT10	51	Digital-Input/Output		VDD	I/O Port
PORT11	52	default input mode			
PORT12	53	Noı	oull-up		
PORT13	54				
SCLK	55	Digital-Input	pull-up	VDD	Serial I/F clock input terminal
SDATA	56	Digital-Input/Output	pull-up	VDD	Serial I/F data input/output terminal
SDEN	57	Digital-Input	pull-up	VDD	Serial I/F enable input terminal
MRSTB	58	Digital-Input	pull-up	VDD	Master reset (reversal) input terminal
VDD4	59	Power			Power supply connected terminal(3.3V)(digital)
ВНС	60	External-capacitor re	quired		External capacitor for LPP bottom hold terminal
MIRRHPF	61	External-capacitor re	quired		Terminal to connect Mirror envelope detector HPF
					capacitor
MIRRBOTH	62	External-capacitor re	quired		Terminal to connect Mirror envelope detector bottom hold capacitor
MIRRTOPH	63	External-capacitor re	quired		Terminal to connect Mirror envelope detector top hold capacitor
BOTH	64	External-capacitor re	auired		Terminal to connect envelope bottom hold capacitor
TOPH	65	External-capacitor re	-		Terminal to connect envelope top hold capacitor
GND1	66	Ground			Ground connected terminal
EQOP	67	Differential-Output			RF equalizer differential output terminal
EQON	68				,
VDD1	69	Power			Power supply connected terminal(3.3V)
SUBI/LPPSIG	70	Analog-Input		VDD	ID detecting HPF input terminal/LPP detecting HPF input
	. •	3 ··· •		-	terminal

SUBO/LPPMON 71 Analog-Output	pin Name	pin No.	Type r	nax. voltaç	ge Function
EQFCF 72 External-capacitor required Terminal to connect RF-equalizer fc auto-adjustment external capacitor REFE 73 External-resistor required Terminal to connect RF-equalizer fc setting external resistor AGHPF2 74 External-capacitor required Terminal to connect AGC high pass filter capacitor reduced AGFP 75 AGFU 76 External-capacitor required AGC filter connecting terminal AGFR 77 External-capacitor required VCC1 78 Power Power supply connected terminal(5V) SUMF/SUMF2 79 Analog-Input / External-capacitor required VDD SUM RF input/SUM differential amp. DC filter connected terminal RFIP 80 Differential-Input VDD RF differential input terminal RFIP 81 SEXEMPLE 82 Analog-Input VDD DSP supply voltage (3.3V) input terminal FVREFO 83 Analog-Output 2.5V reference bias voltage output terminal RFFT 84 External-resistor required Terminal to connect reference current setting external resistor VREF1 85 Analog-Output 2.1V reference bias voltage output terminal HAVC 86 Analog-Input VCC Pickup reference voltage input terminal HAVC 86 Analog-Input VCC Sub beam 4D input terminal SA 87 Analog-Input VCC Sub beam 4D input terminal SC 89 Analog-Input VDD 90 Analog-Input VCC Main beam 4D input terminal MB 93 Analog-Input MC 94 Analog-Input MC 94 Analog-Input MC 94 Analog-Input MC 94 Analog-Input MC 95 Analog-Input MC 96 Ground Ground connected terminal AIN1 97 Analog-Input AIN2 98 Analog-Input AIN3 99 Analog-Input	SUBO/LPPMON	71	Analog-Output		ID detecting HPF output terminal/LPP detecting HPF
REFE 73 External-resistor required Terminal to connect RF-equalizer fc setting external resistor AGHPF2 74 External-capacitor required Terminal to connect AGC high pass filter capacitor reduced AGHPF1 75 AGFU 76 External-capacitor required AGC filter connecting terminal AGFR 77 External-capacitor required VCC1 78 Power Power supply connected terminal(5V) SUMF/SUMF2 79 Analog-Input /External-capacitor required VDD SUM RF input/SUM differential amp. DC filter connecting terminal RFIP 80 Differential-Input VDD SP supply voltage (3.3V) input terminal RFIP 81 SEXPREF 82 Analog-Input VDD DSP supply voltage (3.3V) input terminal RFIP 83 Analog-Input VDD DSP supply voltage (3.3V) input terminal RFIFT 84 External-resistor required Terminal to connect reference current setting external resistor VREF1 85 Analog-Input VCC Pickup reference bias voltage output terminal HAVC 86 Analog-Input VCC Pickup reference voltage input terminal SSR 88 88 Analog-Input VCC Sub beam 4D input terminal SSR 88 88 Analog-Input VCC Main beam 4D input terminal SSR 99 Analog-Input VCC Main beam 4D input terminal MD 95 Analog-Input MC 94 Analog-Input MC 94 Analog-Input MD 95 Analog-Input MC 94 Analog-Input MC 95 Analog-Input MC 96 Ground Ground connected terminal AIN1 97 Analog-Input AIN2 98 Analog-Input AIN3 99 Analog-Input AIN3 99 Analog-Input					output terminal
IREFE 73 External-resistor required Terminal to connect RF-equalizer fc setting external resistor AGHPF2 74 External-capacitor required Terminal to connect AGC high pass filter capacitor AGFP 75 AGFP 75 External-capacitor required AGC filter connecting terminal AGFR 77 External-capacitor required AGC filter connecting terminal AGFR 77 External-capacitor required VCC1 78 Power Power supply connected terminal(5V) SUMF/SUMF2 79 Analog-Input /External-capacitor required VDD SUM RF input/SUM differential amp. DC filter connected terminal RFIP 80 Differential-Input VDD RF differential input terminal RFIP 81 SEVREF 82 Analog-Input VDD DSP supply voltage (3.3V) input terminal FVREFO 83 Analog-Output 2.5V reference bias voltage output terminal IREFT 84 External-resistor required Terminal to connect reference current setting external resistor VREF1 85 Analog-Output VCC Pickup reference voltage input terminal HAVC 86 Analog-Input VCC Sub beam 4D input terminal SA 87 Analog-Input VCC Sub beam 4D input terminal SB 88 Analog-Input VCC Main beam 4D input terminal MA 92 Analog-Input MC 94 Analog-Input MC 94 Analog-Input MC 94 Analog-Input MD 95 Analog-Input MD 95 Analog-Input MD 96 Ground Ground connected terminal AIN1 97 Analog-Input AIN2 98 Analog-Input AIN3 99 Analog-Input	EQFCF	72	External-capacitor required		Terminal to connect RF-equalizer fc auto-adjustment
AGHPF2 74 External-capacitor required 75 AGHPF1 75 AGFU 76 External-capacitor required 76 AGHPF1 75 AGFU 76 External-capacitor required 77 External-capacitor required 77 External-capacitor required 77 External-capacitor required 78 Power 79 Power supply connected terminal (5V) SUMF/SUMF2 79 Analog-Input/ /External-capacitor required 70 SUM RF input/SUM differential amp. DC filter connected terminal 88 Power 80 Differential-Input 70 SUM RF differential input terminal 89 Power 80 Differential-Input 80 Differential-Input 80 DSP supply voltage (3.3V) input terminal 80 Power 82 Analog-Input 83 Analog-Output 84 External-resistor required 85 Analog-Output 85 Analog-Output 85 Analog-Input 86 Analog-Input 87 Power 87 Analog-Input 87 Power 88 Analog-Input 88 Analog-Input 89 Analog-Input 80 Power Supply connected terminal 89 Analog-Input 80 Power Supply					external capacitor
AGHPF2 74 External-capacitor required 75 AGFU 76 External-capacitor required 77 AGFU 76 External-capacitor required 77 AGFU 77 External-capacitor required 77 AGFU 77 External-capacitor required 77 AGFU 78 Power 79 Analog-Input / External-capacitor required 79 Analog-Input / External-capacitor required 70 SUMF/SUMF2 79 Analog-Input / External-capacitor required 70 SUMF/SUMF2 79 Analog-Input 70 SUMF/SUMF2 79 Power 70 SUMF/SUMF2 79 SUMF2 70 SUMF/SUMF2 79 Power 70 SUMF/SUMF2	IREFE	73	External-resistor required		Terminal to connect RF-equalizer fc setting externa
AGHPF1 75 AGFU 76 External-capacitor required AGFR 77 External-capacitor required VCC1 78 Power Power supply connected terminal (5V) SUMF/SUMF2 79 Analog-Input /External-capacitor required VDD SUM RF input/SUM differential amp. DC filter connected terminal RFIP 80 Differential-Input VDD RF differential input terminal RFIN 81 SRVREF 82 Analog-Input VDD DSP supply voltage (3.3V) input terminal FVREFO 83 Analog-Output 2.5V reference bias voltage output terminal RFFT 84 External-resistor required resistor VREF1 85 Analog-Input VCC Pickup reference voltage input terminal HAVC 86 Analog-Input VCC Pickup reference voltage input terminal SA 87 Analog-Input VCC Sub beam 4D input terminal SCC 89 Analog-Input SC 89 Analog-Input VCD 91 Power Power supply connected terminal(3.3V) MA 92 Analog-Input MC 94 Analog-Input MC 94 Analog-Input MC 94 Analog-Input MD 95 Analog-Input MD 95 Analog-Input MD 97 Analog-Input AIN1 97 Analog-Input AIN2 98 Analog-Input AIN3 99 Analog-Input AIN3 99 Analog-Input AIN3 99 Analog-Input					resistor
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AGFR 77 External-capacitor required VCC1 78 Power Power supply connected terminal(5V) SUMF/SUMF2 79 Analog-Input/ /External-capacitor required VDD SUM RF input/SUM differential amp. DC filter connected terminal RFIP 80 Differential-Input VDD RF differential input terminal RFIN 81 SRVREF 82 Analog-Input VDD DSP supply voltage (3.3V) input terminal FVREFO 83 Analog-Output 2.5V reference bias voltage output terminal IREFT 84 External-resistor required resistor VREF1 85 Analog-Output 2.1V reference bias voltage output terminal HAVC 86 Analog-Input VCC Pickup reference voltage input terminal SA 87 Analog-Input VCC Sub beam 4D input terminal SB 88 Analog-Input SC 89 Analog-Input VDD2 91 Power Power supply connected terminal(3.3V) MA 92 Analog-Input MB 93 Analog-Input MC 94 Analog-Input MC 94 Analog-Input MD 95 Analog-Input MD 95 Analog-Input MD 96 Ground Ground connected terminal AIN1 97 Analog-Input AIN2 98 Analog-Input AIN3 99 Analog-Input	AGHPF1	75			
VCC1 78 Power Power supply connected terminal(5V) SUMF/SUMF2 79 Analog-Input/ /External-capacitor required VDD SUM RF input/SUM differential amp. DC filter connected terminal RFIP 80 Differential-Input VDD RF differential input terminal RFIN 81 SRVREF 82 Analog-Input VDD DSP supply voltage (3.3V) input terminal FVREFO 83 Analog-Output 2.5V reference bias voltage output terminal REFT 84 External-resistor required Terminal connect reference current setting external resistor VREF1 85 Analog-Output 2.1V reference bias voltage output terminal HAVC 86 Analog-Input VCC Pickup reference voltage input terminal SA 87 Analog-Input VCC Sub beam 4D input terminal SB 88 Analog-Input SC 89 Analog-Input VDD2 91 Power Power supply connected terminal(3.3V) MA 92 Analog-Input MB 93 Analog-Input MC 94 Analog-Input MD 95 Analog-Input MD 95 Analog-Input MD 96 Ground Ground connected terminal AIN1 97 Analog-Input AIN2 98 Analog-Input AIN3 99 Analog-Input	AGFU	76	External-capacitor required		AGC filter connecting terminal
SUMF/SUMF2 79 Analog-Input/ /External-capacitor required vDD SUM RF input/SUM differential amp. DC filter connected terminal RFIP 80 Differential-Input vDD RF differential input terminal RFIN 81 SRVREF 82 Analog-Input vDD DSP supply voltage (3.3V) input terminal FVREFO 83 Analog-Output 2.5V reference bias voltage output terminal IREFT 84 External-resistor required Terminal to connect reference current setting external resistor VREF1 85 Analog-Output 2.1V reference bias voltage output terminal HAVC 86 Analog-Input VCC Pickup reference voltage input terminal SA 87 Analog-Input VCC Sub beam 4D input terminal SC 89 Analog-Input SC 89 Analog-Input VDD 90 Analog-Input VCC Main beam 4D input terminal MA 92 Analog-Input MC 94 Analog-Input MC 94 Analog-Input MC 94 Analog-Input MD 95 Analog-Input MD 95 Analog-Input AIN1 97 Analog-Input AIN2 98 Analog-Input AIN3 99 Analog-Input	AGFR	77	External-capacitor required		
RFIP 80 Differential-Input VDD RF differential input terminal RFIN 81 SRVREF 82 Analog-Input VDD DSP supply voltage (3.3V) input terminal FVREFO 83 Analog-Output 2.5V reference bias voltage output terminal IREFT 84 External-resistor required Terminal to connect reference current setting external resistor VREF1 85 Analog-Input VCC Pickup reference voltage input terminal HAVC 86 Analog-Input VCC Sub beam 4D input terminal SA 87 Analog-Input VCC Sub beam 4D input terminal SC 89 Analog-Input SC 89 Analog-Input VDD2 91 Power Power supply connected terminal(3.3V) MA 92 Analog-Input MB 93 Analog-Input MC 94 Analog-Input MC 94 Analog-Input MC 95 Analog-Input MD 95 Analog-Input MD 95 Analog-Input MD 95 Analog-Input AlN1 97 Analog-Input AlN1 97 Analog-Input AlN2 98 Analog-Input AlN2 98 Analog-Input AlN3 99 Analog-Input AlN3 99 Analog-Input AlN3 99 Analog-Input	VCC1	78	Power		Power supply connected terminal(5V)
RFIP 80 Differential-Input VDD RF differential input terminal RFIN 81 SRVREF 82 Analog-Input VDD DSP supply voltage (3.3V) input terminal FVREFO 83 Analog-Output 2.5V reference bias voltage output terminal IREFT 84 External-resistor required Terminal to connect reference current setting external resistor VREF1 85 Analog-Output 2.1V reference bias voltage output terminal HAVC 86 Analog-Input VCC Pickup reference voltage input terminal SA 87 Analog-Input VCC Sub beam 4D input terminal SB 88 Analog-Input SC 89 Analog-Input SD 90 Analog-Input VDD2 91 Power Power supply connected terminal(3.3V) MA 92 Analog-Input MB 93 Analog-Input MC 94 Analog-Input MD 95 Analog-Input MD 95 Analog-Input MD 95 Analog-Input AIN1 97 Analog-Input AIN2 98 Analog-Input AIN2 98 Analog-Input AIN3 99 Analog-Input	SUMF/SUMF2	79	Analog-Input/ /External-capacitor required	VDD	SUM RF input/SUM differential amp. DC filte
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IREFT 84 External-resistor required Terminal to connect reference current setting external resistor VREF1 85 Analog-Output 2.1V reference bias voltage output terminal HAVC 86 Analog-Input VCC Pickup reference voltage input terminal SA 87 Analog-Input VCC Sub beam 4D input terminal SB 88 Analog-Input SC 89 Analog-Input SD 90 Analog-Input VDD2 91 Power Power supply connected terminal(3.3V) MA 92 Analog-Input MB 93 Analog-Input MC 94 Analog-Input MD 95 Analog-Input MD 95 Analog-Input GND2 96 Ground Ground connected terminal AIN1 97 Analog-Input AIN2 98 Analog-Input AIN3 99 Analog-Input AIN3 PC 2.1V reference current setting external resistor Cannot connect reference current setting external resistor Cannot connected terminal Terminal to connected terminal VCC Bickup reference current setting external resistor Cannot connected terminal Terminal to connected terminal Terminal to connected terminal Terminal to connected terminal	SRVREF	82	Analog-Input	VDD	DSP supply voltage (3.3V) input terminal
VREF1 85 Analog-Output 2.1V reference bias voltage output terminal HAVC 86 Analog-Input VCC Pickup reference voltage input terminal SA 87 Analog-Input VCC Sub beam 4D input terminal SB 88 Analog-Input SC 89 Analog-Input SD 90 Analog-Input VDD2 91 Power Power supply connected terminal(3.3V) MA 92 Analog-Input MB 93 Analog-Input MC 94 Analog-Input MD 95 Analog-Input MD 95 Analog-Input GND2 96 Ground Ground connected terminal AIN1 97 Analog-Input AIN2 98 Analog-Input AIN3 99 Analog-Input AIN3 99 Analog-Input AIN3 99 Analog-Input AIN3 99 Analog-Input AIN4 VCD Analog input terminal AIN5 Analog-Input AIN6 Analog-Input AIN7 Analog-Input AIN8 99 Analog-Input AIN8 99 Analog-Input AIN9 Analog-Input	FVREFO	83	Analog-Output		2.5V reference bias voltage output terminal
VREF1 85 Analog-Output 2.1V reference bias voltage output terminal HAVC 86 Analog-Input VCC Pickup reference voltage input terminal SA 87 Analog-Input VCC Sub beam 4D input terminal SB 88 Analog-Input SC 89 Analog-Input SD 90 Analog-Input VDD2 91 Power Power supply connected terminal(3.3V) MA 92 Analog-Input VCC Main beam 4D input terminal MB 93 Analog-Input MC 94 Analog-Input MD 95 Analog-Input GND2 96 Ground Ground connected terminal AIN1 97 Analog-Input AIN2 98 Analog-Input AIN3 99 Analog-Input AIN3 99 Analog-Input	IREFT	84	External-resistor required		Terminal to connect reference current setting externa
HAVC 86 Analog-Input VCC Pickup reference voltage input terminal SA 87 Analog-Input VCC Sub beam 4D input terminal SB 88 Analog-Input SC 89 Analog-Input SD 90 Analog-Input VDD2 91 Power Power supply connected terminal(3.3V) MA 92 Analog-Input MB 93 Analog-Input MC 94 Analog-Input MD 95 Analog-Input GND2 96 Ground Ground connected terminal AIN1 97 Analog-Input AIN2 98 Analog-Input AIN3 99 Analog-Input					resistor
SA 87 Analog-Input VCC Sub beam 4D input terminal SB 88 Analog-Input SC 89 Analog-Input SD 90 Analog-Input VDD2 91 Power Power supply connected terminal(3.3V) MA 92 Analog-Input WB 93 Analog-Input MC 94 Analog-Input MD 95 Analog-Input GND2 96 Ground Ground connected terminal AIN1 97 Analog-Input AlN2 98 Analog-Input AlN3 99 Analog-Input AlN3 99 Analog-Input AlN3 99 Analog-Input AlN3 99 Analog-Input	VREF1	85	Analog-Output		2.1V reference bias voltage output terminal
SB 88 Analog-Input SC 89 Analog-Input SD 90 Analog-Input VDD2 91 Power Power supply connected terminal(3.3V) MA 92 Analog-Input MB 93 Analog-Input MC 94 Analog-Input MD 95 Analog-Input GND2 96 Ground Ground connected terminal AIN1 97 Analog-Input AIN2 98 Analog-Input AIN3 99 Analog-Input	HAVC	86	Analog-Input	VCC	Pickup reference voltage input terminal
SC 89 Analog-Input SD 90 Analog-Input VDD2 91 Power Power supply connected terminal(3.3V) MA 92 Analog-Input VCC Main beam 4D input terminal MB 93 Analog-Input MC 94 Analog-Input MD 95 Analog-Input GND2 96 Ground Ground connected terminal AIN1 97 Analog-Input VDD Analog input terminal AIN2 98 Analog-Input AIN3 99 Analog-Input	SA	87	Analog-Input	VCC	Sub beam 4D input terminal
SD 90 Analog-Input VDD2 91 Power Power supply connected terminal(3.3V) MA 92 Analog-Input MB 93 Analog-Input MC 94 Analog-Input MD 95 Analog-Input GND2 96 Ground Ground connected terminal AIN1 97 Analog-Input AIN2 98 Analog-Input AIN3 99 Analog-Input	SB	88	Analog-Input		
VDD2 91 Power Power supply connected terminal(3.3V) MA 92 Analog-Input VCC Main beam 4D input terminal MB 93 Analog-Input MC 94 Analog-Input MD 95 Analog-Input GND2 96 Ground Ground connected terminal AIN1 97 Analog-Input AIN2 98 Analog-Input AIN3 99 Analog-Input	SC	89	Analog-Input		
MA 92 Analog-Input VCC Main beam 4D input terminal MB 93 Analog-Input MC 94 Analog-Input MD 95 Analog-Input GND2 96 Ground Ground connected terminal AIN1 97 Analog-Input AIN2 98 Analog-Input AIN3 99 Analog-Input	SD	90	Analog-Input		
MB 93 Analog-Input MC 94 Analog-Input MD 95 Analog-Input GND2 96 Ground Ground connected terminal AIN1 97 Analog-Input AIN2 98 Analog-Input AIN3 99 Analog-Input	VDD2	91	Power		Power supply connected terminal(3.3V)
MC 94 Analog-Input MD 95 Analog-Input GND2 96 Ground Ground connected terminal AIN1 97 Analog-Input VDD Analog input terminal AIN2 98 Analog-Input AIN3 99 Analog-Input	MA	92	Analog-Input	VCC	Main beam 4D input terminal
MD 95 Analog-Input GND2 96 Ground Ground connected terminal AIN1 97 Analog-Input VDD Analog input terminal AIN2 98 Analog-Input AIN3 99 Analog-Input	МВ	93	Analog-Input		
GND2 96 Ground Ground connected terminal AIN1 97 Analog-Input VDD Analog input terminal AIN2 98 Analog-Input AIN3 99 Analog-Input	MC	94	Analog-Input		
AIN1 97 Analog-Input VDD Analog input terminal AIN2 98 Analog-Input AIN3 99 Analog-Input	MD	95	Analog-Input		
AIN2 98 Analog-Input AIN3 99 Analog-Input	GND2	96	Ground		Ground connected terminal
AIN3 99 Analog-Input	AIN1	97	Analog-Input	VDD	Analog input terminal
<u> </u>	AIN2	98	Analog-Input		
SIGM 100 Analog-Output Analog signal monitoring output terminal	AIN3	99	Analog-Input		
	SIGM	100	Analog-Output		Analog signal monitoring output terminal

IC301 (R8J32007FPV) : Encoder, Decoder & DSP Singal Processor 1.1 Pin Layout



1.2 Block Diagram



1.3 Pin Table

Pin no	Pin Name
1	VSSR
2	VCCR
3	CPU14
4	CPU13
5	CPU12
6	VSSIO
7	VCCIO
8	VCCRQ
9	CPU11
10	CPU10
11	VSSRQ
12	CPU9
13	CPU8
14	CPRDB
15	USC0B
16	A1
17	CPU0
18	CPU1
19	CPU2
20	CPU3
21	CPU4
22	VSSRQ
23	CPU5
24	CPU6
25	CPU7
26	VCCRQ
27	VSS
28	VDD
29	A16
30	A15
31	VSSIO
32	VCCIO
33	A14
34	A13
35	A12
36	A11
37	A10
38	A9
39	A20
40	CPWRB
41	VDD
42	VSS
43	A19
44	A18
45	A18
46	
	A7
47	A6
48	A5
49	A4
50	A3
51	VSSIO
52	VCCIO
53	VCCR
54	VSSR

Pin no	Pin Name
55	A2
56	GPIO05
57	VSSIO
58	VCCIO
59	HRSTB
60	DATA7
61	DATA8
62	DATA6
63	DATA9
64	DATA5
65	DATA10
66	DATA4
67	DATA11
68	DATA3
69	DATA12
70	DATA2
71	DATA13
72	VDD
73	VSS
74	VSSIO
75 70	VCCIO
76	DATA1
77	DATA14
78	DATA0
79	DATA15
80	DREQ
81	ZIONB
82	ZIORB
83	IORDY DACKB
84	HINTRQ
85 86	IOCS16B
87	VSSIO
88	VCCIO
89	DA1
90	PDIAGB
91	DA0
92	DA2
93	CS1FXB
94	CS3FXB
95	DASPB
96	CPIO07
97	CPIO06
98	ROUT
99	VCCA
100	LOUT
101	ADIPVR1
102	ADIPVRT
103	ADIPINP
104	VSSA
105	VSSA
106	XCO
107	XCI
108	VCCA
,	,

Pin no	Pin Name
109	DOUT
110	TEST0
111	TEST1
112	TEST2
113	TEST3
114	TMS
115	TCK
116	TDI
117	TDO
118	TRST
119	FEMCK
120	SCLK
121	SDATA
122	RFDEN
123	WDEN
124	LDBUSY
125	TCSHSPBLV
126	RFPDSH
127	WFPDSH
128	MPDSH WBLSH
129	VDD
130 131	VSS
132	VSSIO
133	VCCIO
134	WRGATE2
135	WRSTOP
136	SRFL
137	SRFH
138	WRGATEB
139	VCCA
140	DCLK
141	DCLKB
142	NRZIB
143	NRZI
144	VSSA
145	VSS
146	VDD
147	VSSIO
148	VCCIO
149	IP2MIRR
150	IP1LPPIN
151	RFHLD
152	IDGATE
153	LOWZB
154	WOBSIG
155	LNDTRK
156	BLANK
157	DEFECT
158	VSSAA
159	VDDAA
160	W2LPF2
161	W2LPF1
162	W2LPF0

Pin no	Pin Name
163	W1LPF2
164	W1LPF1
165	W1LPF0
166	VCCA
167	VSSA
168	VSSA
169	FE
170	PE
171	SIGM
172	ATZC
173	TE
174	LPSA
175	TCPH
176	TIBH
177	BCENT
178	GAD0
179	GAD0
180	FOD
181	TRD
182	TVDP
183	TVDN
184	
	DAVC
185	VCCA
186	VCCA
187	VSSA
188	VINN
189	VDDAA
190	VINP
191	VSSA
192	PTEST1
193	VDDAA
194	REXT
195	VSSA
196	PTEST2
197	VDDAA
198	PTEST3
199	VCC
200	VCCIO
201	VSSIO
202	MRSTB
203	TESTB2
204	TESTB1
205	ICUIN7
206	ICUIN6
207	ICUIN8
208	GPIO04
209	LED
210	LDD
211	SPD
212	TLD
213	SFG
214	EFG
215	A17
216	CPU15

1.4 Pin Functions

It corresponds to the following signs as a pin I/O specification.

AI: Analog Input IOU: Standard Input/Output with Pull Up

AO: Analog Output 5I: 5V Tolerant Input AIO: Analog Input/Output 5O: 5V Tolerant Output

I: Standard Input 5TO: 5V Tolerant Three State Output IU: Standard Input with Pull Up 5IO: 5V Tolerant Input/Output

O: Standard Output PW: Power Supply Pin

TO: Standard Three State Output GND: Earth Pin

IO: Standard Input/Output

Data PLL/PRML Pin List

Pin Name	Pin No.	1/0	destination	Function
VINP	190	ΑI	AFE	RF signal normal phase input pin
VINN	188			RF signal counter phase input pin
REXT	194	AO	External Resistance	Resistor connect pin for reference current generation
PTEST1	192	AO	External Resistance	PRML/Data PLL moniter D/A output pin
PTEST2	196			PRML/Data PLL moniter D/A output pin
PTEST3	198			Data PLL VCO control voltage monitor pin

WpII Pin List

Pin Name	Pin No.	I/O	destination	Function
W1LPF0	165	AO	External Components	Write PLL1 filter connect pin (0)
W1LPF1	164			Write PLL1 filter connect pin (1)
W1LPF2	163			Write PLL1 filter connect pin (2)
W2LPF0	162	AO	External Components	Write PLL2 filter connect pin (0)
W2LPF1	161			Write PLL2 filter connect pin (1)
W2LPF2	160			Write PLL2 filter connect pin (2)

Servo Pin List

Pin Name	Pin No.	I/O	destination	Function
BLANK	156		AFE	Blank signal input
				(also connected to the H8S interrupt port INT5)
DEFECT	157	ı	AFE	Defect (scratch detect) signal
SFG	213	IU	DRVR	Spindle FG pulse
				(also input to the H8S interrupt port INT4)
EFG	214	ı	PU	Spindle FG pulse for Light Scribe
				(also input to the H8S interrupt port INT4)
TLD	212	TO	DRVR	Tilt drive signal (PWM output)
SPD	211	TO	DRVR	Spindle drive signal (PWM output)
LDD	210	TO	DRVR	Loading drive signal (PWM output)
LED	209	TO	PU	LPS_LED control signal (PWM output)
ATZC	172	ΑI	AFE	Tracking Zero Cross input signal
FE	169	ΑI	AFE	Focus error: sampled at 352.8 kHz
PE	170	ΑI	AFE	Laser power error: sampled at 352.8 kHz
SIGM	171	ΑI	AFE	Signal monitor: sampled at 88.2/176.4 kHz
TE	173	ΑI	AFE	Tracking error: sampled at 352.8 kHz
LPSA	174	ΑI	AFE	Lens positioning/lens error: sampled at 88.2 kHz
TCPH	175	Al	AFE	Tracking center/BETA top hold: sampled at 44.1/176.4 kHz
TIBH	176	Al	AFE	Tilt error/BETA bottom hold: sampled at 44.1/176.4 kHz
BCENT	177	Al	AFE	BETA center: sampled at 176.4 kHz
GAD1	179	Al		General AD input: sampled at 88.2 kHz
GAD0(VRDC2N)	178	Al		General AD input: sampled at 176.4 kHz
FOD	180	AO	DRVR	Focus control signal
TRD	181	AO	DRVR	Tracking control signal
TVDP	182	AO	DRVR	Sled drive signal (normal phase)
TVDN	183			Sled drive signal (counter phase)
DAVC	184	AO	DRVR	Servo system Vcc/2 voltage output pin

ATAPI Interface Pin List

Pin Name	Pin No.	I/O	destination	Function
HRSTB	59	51	ATAPI	ATAPI-IF control signal (host reset signal)
DA2	92	51	ATAPI	ATAPI-IF register address signal
DA1	89			
DA0	91			
DATA[15:0]	79,77,71,	5IO	ATAPI	ATAPI- IF data bus
	69,67,65,			
	63,61,60,			
	62,64,66,			
	68,70,76,			
	78			
DREQ	80	5TO	ATAPI	ATAPI-IF DMA request signal
ZIOWB	81	51	ATAPI	ATAPI-IF write strobe pulse
ZIORB	82	51	ATAPI	ATAPI-IF read strobe pulse
IORDY	83	5TO	ATAPI	ATAPI-IF control signal (drive Ready)
DACKB	84	51	ATAPI	ATAPI-IF DMA acknowledge
HINTRQ	85	5TO	ATAPI	ATAPI-IF drive interrupt signal
IOCS16B	86	5TO	ATAPI	ATAPI-IF control signal (16-bit transfer)
PDIAGB	90	5IO	ATAPI	ATAPI-IF control signal
CS1FXB	93	51	ATAPI	ATAPI-IF register chip select signal
CS3FXB	94			
DASPB	95	5IO	ATAPI	ATAPI-IF control signal

Encoder Interface Pin List

Pin Name	Pin No.	I/O	destination	Function		
IP1LPPIN	150	I	AFE	PID area identification signal/LPP input signal		
IP2MIRR	149	I	AFE	PID area identification signal/MIRR signal		
WOBSIG	154	I	AFE	Wobble signal input		
LOWZB	153	0	AFE	Input impedance switch control signal/SPDSH; running OPC sampling pulse (Pit top)		
IDGATE	152	0	AFE	ID/data switch signal		
RFHLD	151	0	AFE	VFO3 holding signal and track center signal sample & hold signal		
WRGATE2	134	0	AFE	Write gate signal output		
WBLSH	129	0	AFE	Wobble signal sampling pulse		
MPDSH	128	0	AFE	Main beam sampling pulse		
WFPDSH	127	0	AFE	Laser control sampling pulse (Front monitor write/erase block)		
RFPDSH	126	0	AFE	Laser control sampling pulse (Front monitor read block)		
TCSHSPBLV	125	0	AFE	VFO1 track center signal sample & hold pulse; /SPBLVL running OPC sampling pulse (Pit end)		
WRGATEB	138	0	PU	Write gate signal		
SRFH	137	0	PU	I- V amplifier gain switch (HI side) /I- V amplifier gain switch (for binary)		
SRFL	136			I- V amplifier gain switch (Low side)		
WRSTOP	135	ı	PU	Write stop gate signal		
LNDTRK	155	0	AFE/PU	Land/groove switch		
NRZI	143	AO	PU	NRZI output after modulation (normal phase)		
NRZIB	142			NRZI output after modulation (counter phase)		
DCLK	140	AO	PU	NRZI sync clock (counter phase)		
DCLKB	141			NRZI sync clock (normal phase)		
ADIPVR1	101	AO	External Cpmponents	AD related pin for ADIP detection		
ADIPVRT	102	AO	External Cpmponents	AD related pin for ADIP detection		
ADIPINP	103	Al	AFE	ADIP detect input pin		

Serial Communication Interface Pin List

Pin Name	Pin No.	I/O	destination	Function	
LDBUSY	124	Ю	LDD	LDD serial IF busy also functions as the CPU general port 1-0	
WDEN	123	0	LDD	LDD microcomputer I/F (transfer enable signal)	
RFDEN	122	0	AFE	AFE microcomputer I/F (transfer enablesignal)	
SDATA	121	Ю	AFE/LDD	AFE/LDD microcomputer I/F (transfer data signal 3Vsystem)	
SCLK	120	0	AFE/LDD	AFE/LDD microcomputer I/F (transfer clock signal)	

Audio Interface Pin List

Pin Name	Pin No.	I/O	destination	Function	
DOUT	109	Ю	ATAPI	Digital output pin,also functions as the CPU general port 1-2	
ROUT	98	AO	ATAPI	Audio Lch & Rch output	
LOUT	100				

Clock Generator Pin List

Pin Name	Pin No.	I/O	destination	Function	
FEMCK	119	0	AFE	Front End LSI clock	
XCO	106	0	X'tal	Crystal oscillation 33.8688MHz	
XCI	107	I	X'tal	Crystal oscillation 33.8688MHz	

H8S Micro-Processor Pin List CPU

Pin Name	Pin No.	I/O	destination	Function		
ICUIN7(ACTFLG)	205	IU	DRVR	CPU interrupt port INT7: Pick up protect flag		
ICUIN6(EJECTSW)	206	I	Eject Switch	Eject Switch CPU interrupt port INT6: EJECTSW interrupt request		
ICUIN8(LOADIN)	207	Ю	Load Switch	witch CPU general port1-1 also connected to the CPU interrupt		
				port INT8: Loader in sensor		
GPIO07(HEATRUN)	96	5IO	ATAPI	CPU general port 0-7 :Off heat run test input		
GPIO06(CSEL)	97	5IO	ATAPI	CPU general port 0-6 ATAPI CSEL		
GPIO04(A0)	208	Ю	SRAM	CPU general port 0-4, also functions as H8S / A0		
GPIO05(UCS1B)	56	Ю	SRAM	CPU general port 0-5, also functions as H8S / CS1		

Flash/SRAM Pin List

Pin Name	Pin No.	I/O	destination	Function		
UCS0B	15	0	Flash	H8S / CS0		
CPWRB	40	0	Flash / SRAM	H8S / WRB		
CPRDB	14	0	Flash / SRAM	H8S / RDB		
A[20:1]	39,43,44,	0	Flash / SRAM	H8S / A[20:1]		
	215,29,30,					
	33,34,35,					
	36,37,38,					
	45,46,47,					
	48,49,50,					
	55,16					
CPU[15:1]	216,3,4,	Ю	Flash / SRAM	H8S / D[15:0]		
	5,9,10,			CPU[0] can also function as the CPU general port 0-4		
				(multiplexed).		
	12,13,25,					
	24,23,21,					
	20,19,18					
	17					

LSI/TEST Control Pin List

Pin Name	Pin No.	I/O	destination	Function	
MRSTB	202	I	RESET IC	Master reset input	
TESTB2	203	-		Test select	
TESTB1	204				
TMS	114	IU	E10emulator	Test data switch for E10emulator	
TCK	115	IOU	E10emulator	Test clock for E10 emulator	
				It can function as a SCI serial clock output port when E10	
				emulator is not used (multiplexed).	
TDI	116	IU	E10emulator	Test data input for E10 emulator	
				It can function as a SCI serial data input port when E10	
				emulator is not used (multiplexed).	
TDO	117	0	E10emulator Test data output for E10 emulator		
				It can function as a SCI serial data output port when E10	
				emulator is not used (multiplexed).	
TRST	118	I	E10emulator	lator Test reset for E10 emulator	
				/Non-mask CPU interrupt port(falling edge sense)	
TEST0	110	O	User test/CPU general port2		
TEST1	111			Test monitor can be set as the following table by a register	
TEST2	112				
TEST3	113				

T*SEL[3:0]	TEST0	TEST1	TEST2	TEST3
0	Servo monitor 0	Servo monitor 1	Servo monitor 2	Servo monitor 3
1	WPLL monitor 0	WPLL monitor 1	WPLL monitor 2	WPLL monitor 3
2	Audio 0	Audio 1	Audio 2	Audio 3
3	DVD modulation 0	DVD modulation 1	DVD modulation 2	DVD modulation 0
4	DVD-R/CD-R monitor 0	DVD-R/CD-R monitor1	DVD-R/CD-R monitor 2	DVD-R/CD-R monitor 3
5	DVD+RW monitor 0	DVD+RW monitor1	DVD+RW monitor 2	DVD+RW monitor 3
6	PI/C1	PI/C1	PI/C1	PI/C1
7	PO/C2	PO/C2	PO/C2	PO/C2
8	DEMO 0	DEMO 1	DEMO 2	DEMO 3
9	-	-	•	-
10	CLVCK	CLVCK	CLVCK	CLVCK
11	BLEND	BLEND	BLEND	BLEND
12	PRML monitor 0	PRML monitor 1	PRML monitor 2	PRML monitor 3
13	Data PLL monitor 0	Data PLL monitor 1	Data PLL monitor 2	Data PLL monitor 3
14	RAMCON monitor 0	RAMCON monitor 1	RAMCOM monitor 2	RAMCON monitor 3
15	MIF monitor 0	MIF monitor 1	MIF monitor 2	MIF monitor 3
16	WOBREF monitor 0	WOBREF monitor 1	WOBREF monitor 2	WOBREF monitor 3

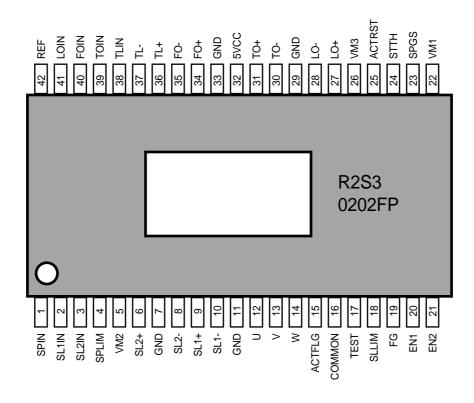
T*SEL can be set for each of pins TEST3, TEST2, TEST1, and TEST0, respectively.

Power Supply/GND Pin List

Pin Name	Pin No.	I/O	Function	
VDD	28,41,72,	PW	DSP core power supply (1.5V)	
	130,146			
VCCR	2,53	PW	SDRAM power supply (3.3V)	
VCCRQ	8,26		SDRAM I/O power supply (3.3V)	
VDDAA	159	PW	1.5V system analog power supply (1.5V) WPLL1,2	
	189,193,197		1.5V system analog power supply (1.5V) PRML A/D Data PLL	
VCCA	99	PW	Analog power supply (3.3V):AUDIO / ADIP	
	108		Analog power supply (3.3V):PLL multiplication	
	139		Analog power supply (3.3V):LVDS	
	166		Analog power supply (3.3V):WPLL1,2	
	185		Analog power supply (3.3V):Servo A/D D/A	
	186		Analog power supply (3.3V):PRML A/D Data PLL	
VCC	199	PW	Digital power supply (3.3V):PRML A/D Data PLL	
VCCIO	7,32,52,	PW	DSP I/O power supply (3.3V)	
	58,75,88,			
	133,148,200			
VSS	27,42,73,	GND	DSP core GND	
	131,145			
VSSR	1,54	GND	SDRAM GND	
VSSRQ	11,22	GND	SDRAM I/O GND	
VSSA	104	GND	Analog GND:AUDIO / ADIP	
	105		Analog GND:PLL multiplication	
	144		Analog GND:LVDS	
	167		Analog GND:WPLL1,2	
	168		Analog GND:Servo A/D D/A	
	187,191,195		Analog GND:PRML A/D Data PLL	
VSSAA	158	GND	1.5V system analog GND:WPLL1,2	
VSSIO	6,31,51,	GND	DSP I/O GND	
	57,74,87,		Connected SDRAM I/O GND through 6,31pin	
	132,147,201			

IC601 (R2S30202FP): SPINDLE MOTOR AND 6CH ACTUATOR DRIVER

Pin Layout



Package outline: 42 PIN POWER SSOP (42P9R-K)

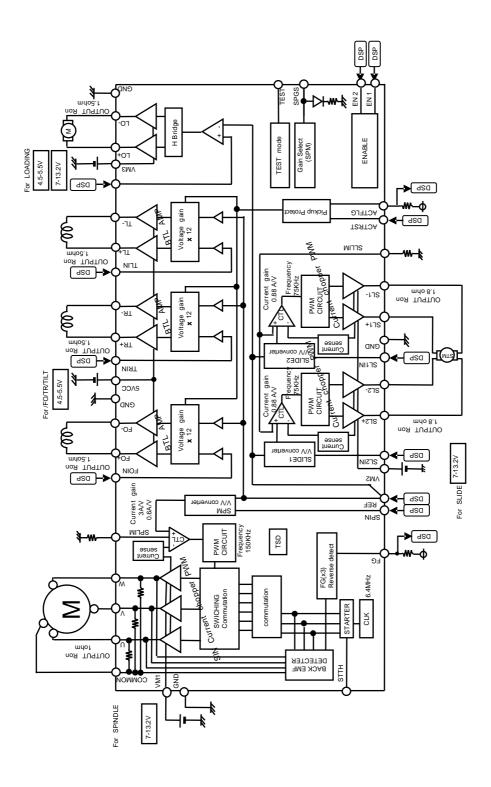
Pin Function

No	Pin name	Function	No	Pin name	Function
1	SPIN	Spindle control voltage input		REF	Reference voltage input
2	SL1IN	Slide control voltage input1	41	LOIN	Loading control input
3	SL2IN	Slide control voltage input2	40	FOIN	Focus control voltage input
4	SPLIM	Input terminal for spindle current limit	39	TOIN	Tracking control voltage input
5	VM2	Motor Power Supply 2(for Slide)	_38	TLIN	Tilt control voltage input
6	SL2+	Slide non-inverted output2	_37	TL-	Tilt inverted output
7	GND	GND	_36	TL+	Tilt non-inverted output
8	SL2-	Slide inverted output2	_ 35	FO-	Focus inverted output
9	SL1+	Slide non-inverted output1	34	FO+	Focus non-inverted output
10	SL1-	Slide inverted outptut1	33	GND	GND
11	GND	GND	32	5VCC	5V Power Supply (for FS,TS,TL)
12	U	Motor drive output U		TO+	Tracking non-inverted output
13	V	Motor drive output V		TO-	Tracking inverted output
14	W	Motor drive output W	29	GND	GND
15	ACTFLG	Pickup protect flag output	28	LO-	Loading inverted outptut
16	COMMON	Motor common	_27	LO+	Loading non-inverted output
17	TEST	Test terminal (*1)		VM3	Power Supply3(for Loading)
18	SLLIM	Input terminal for slide current limit		ACTRST	Pickup protect Reset (*2)
19	FG	Frequency generator output		STTH	Reference voltage for spindle start up
20	EN1	Input terminal for enable 1	23	SPGS	Input terminal for gain select SPM
21	EN2	Input terminal for enable 2		VM1	Motor Power Supply 1(for Spindle)

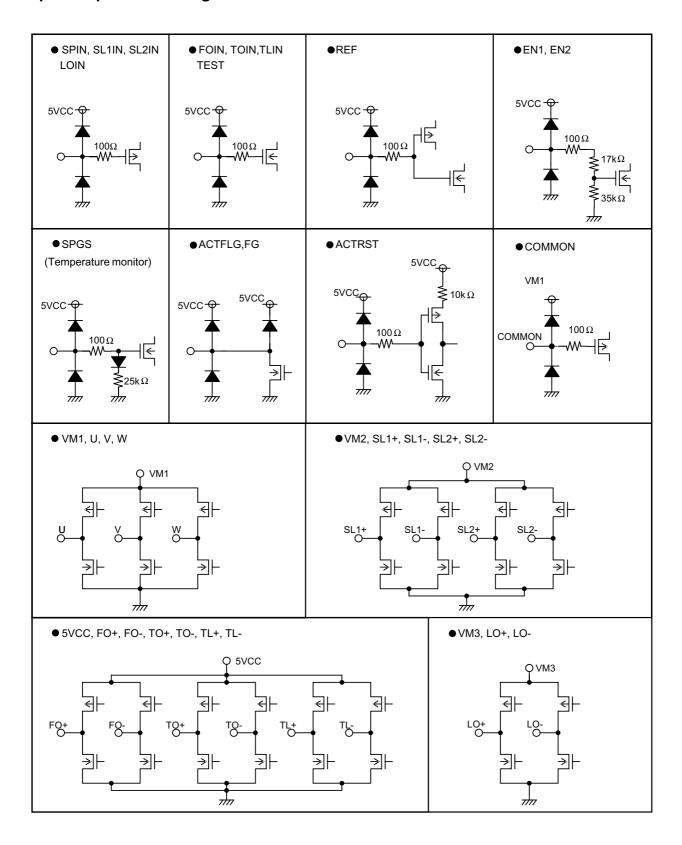
^{*1)} Please connect 17terninal (TEST) to GND or open, for TEST.

^{*2)} Please connect 25terminal(ACTRST) to 5VCC, When the Pick-up protection circuit is not used.

Block Diagram

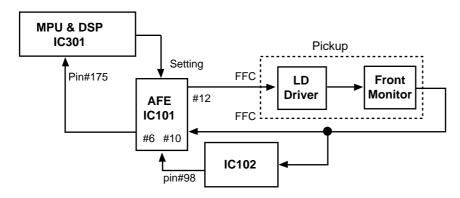


Input/Output circuit diagram

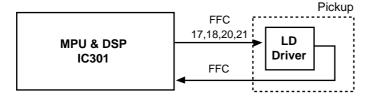


TROUBLESHOOTING GUIDE

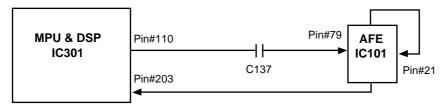
(01) Laser Power Adjust (using RD Power/WR Power/Erase Power)



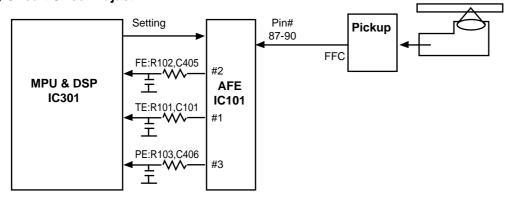
(02) High Frequency/NRZI skew Adjust



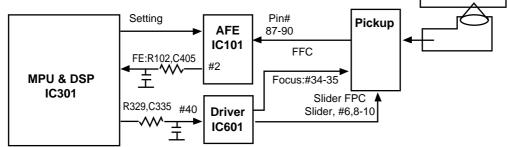
(03) Data Slice/Equalizer Boost/Raw Slice/ Equalizer Frequency Adjust



(04) Circuit Offset Adjust

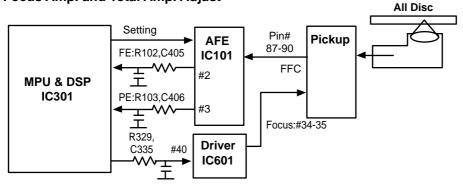




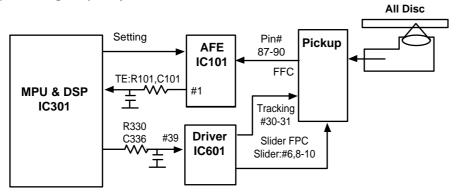


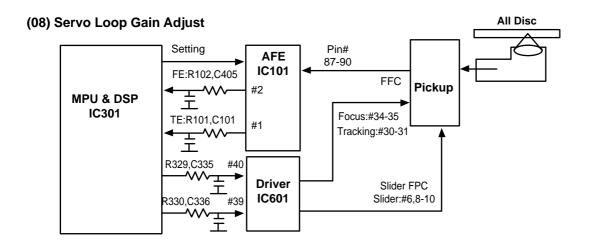
DVD-Dual Disc

(06) Focus Amp. and Total Amp. Adjust

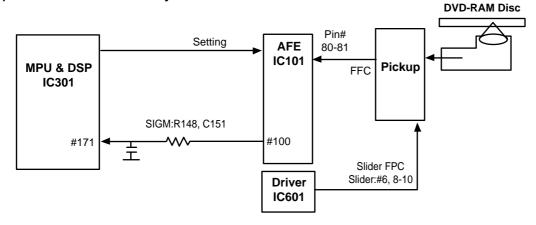


(07) Tracking Amp. Adjust

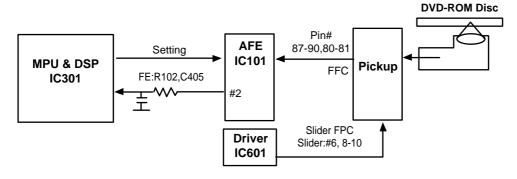




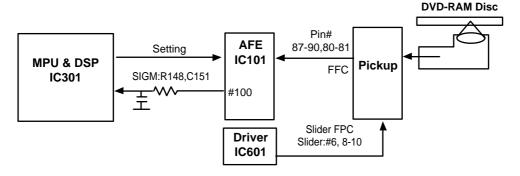
(09) Unwritten Slice Level Adjust for DVD-RAM



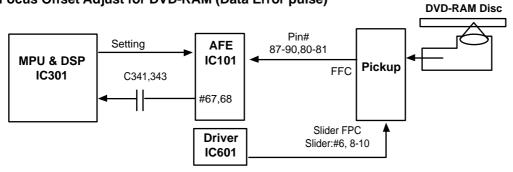
(10) Focus Offset Adjust for DVD-ROM, CD-R/RW



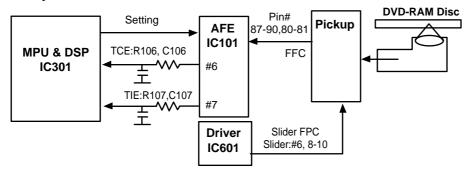
(11) Focus Offset Adjust for DVD-RAM (PID Amp)



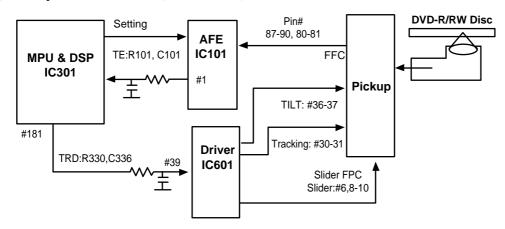




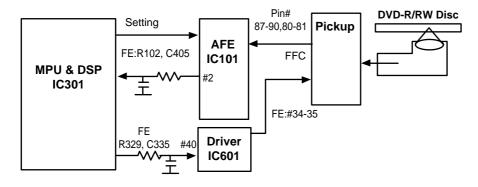
(13) Tilt Adjust for DVD-RAM



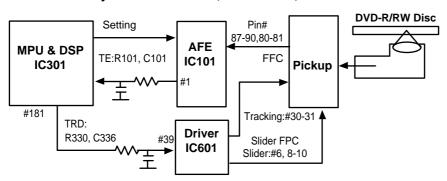
(14) Tilt Adjust for DVD-R/RW, DVD+R/RW, CD-R/RW



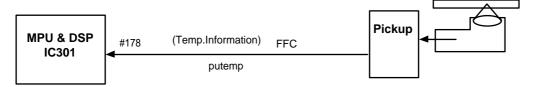
(15) Focus Deviation Adjust



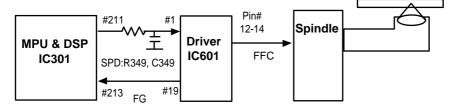
(16) Focus Offset Adjust for DVD-R/RW, DVD+R/RW, CD-R/RW



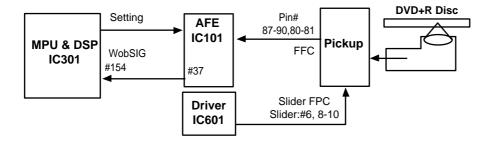
(17) Lens Sensitivity Adjust



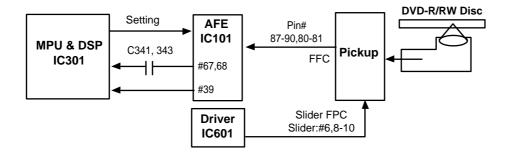
(18) Spindle Offset Adjust



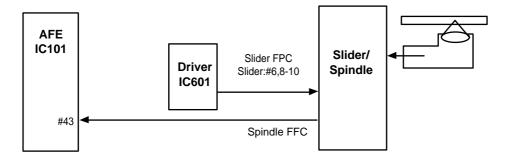
(19) ADIP BPF/Read Timing Adjust for DVD+R/RW



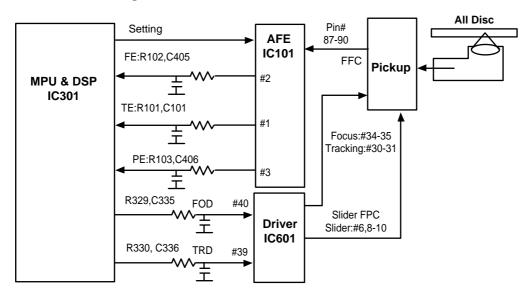
(20) Focus Offset Adjust for DVD-R/RW, DVD+R/RW(DID)



(21) RTZ TimeOut Fail



(22) Focus Servo/Tracking Servo Fail



Detail Error Code & Fail Analysis

1. Laser Power Initial Adjust

No.	Error Code SSB Byte8,9	Contents of fail	Fail Analysis	Block Diagram
1	28xx (Exchange low/high byte) Byte8: xxh Byte9: 28h	LP Adjust NG.	 Check Pickup FFC Connection. Check solder of IC101circumference. (pin#6, 10, 12, L150, L151) Check solder of IC102. Exchange Pickup(LDD, Front Monitor). Exchange IC101(AFE). Exchange IC301(MPU & DSP). 	No.01
2	48xx	High Frequency Adjust NG.	 Check Pickup FFC Connection. Exchange Pickup (LDD part). Exchange IC301(DSP). 	No.02
3	5Exx	NRZi Skew Adjust NG.	1) Check Pickup FFC Connection 2) Exchange Pickup (LDD part). 3) Exchange IC301(MPU & DSP).	No.02
4	4C0x to 4C4x	Data Slice Adjust NG.	 Check solder of IC101circumference. (pin# 79, L150, L151) Exchange IC101(AFE). Exchange IC301(MPU & DSP). 	No.03
5	4C5x to 4C7x	EQ Boost Adjust NG.	 Check solder of IC101circumference. (pin# 79, L150, L151) Exchange IC101(AFE). Exchange IC301(MPU & DSP). 	
6	4C80	RAW Slice Level Adjust NG.	1) Check solder of IC101circumference. (pin# 79, L150, L151) 2) Exchange IC101(AFE). 3) Exchange IC301(MPU & DSP).	
7	4CAx	EQ Auto Frequency Adjust NG	 Check solder of IC101circumference. (pin# 79, L150, L151) Exchange IC101(AFE). Exchange IC301(MPU & DSP). 	

2. Adjusting Error during Disc Load Sequence (Lead in Error)

No.	Error Code SSB Byte21,22	Contents of fail	Fail Analysis	Block Diagram
1	42xx	Circuit Offset Adjust NG.	1) Check Pickup FFC Connection. 2) Check solder of IC101circumference . (pin#,1,2,3 pin#87-90, FE_Servo: R102, C405 TE_Servo: R101, C101 PE_Servo: R103, C406) 3) Exchange IC101(AFE). 4) Exchange Pickup. 5) Exchange IC301(MPU & DSP).	No.04
2	452x	Focus Amp Adjust NG. (DVD-DL Only)	1) Check DVD-Dual Disc. 2) Check Pickup FCC Connection. 3) Check solder of IC101circumference. (pin#1,2,3 pin#87-90, FE_Servo: R102, C405) 4) Check Slider FPC Connection. 5) Exchange IC101(AFE). 6) Exchange IC601(Driver). 7) Exchange IC301(MPU & DSP).	No.05
3	450x 451x 454x	Focus Amp Adjust NG. Total Amp Adjust NG.	1) Check Pickup FFC Connection. 2) Check solder of IC101circumference. (pin#1,2,3 pin#87-90, FE_Servo: R102, C405 PE_Servo: R103, C406) 3) Exchange Pickup. 4) Exchange IC101(AFE). 5) Exchange IC301(MPU & DSP).	No.06
4	458x	Tracking Amp Adjust NG.	1) Check Pickup FFC Connection. 2) Exchange Pickup. 3) Check solder of IC101circumference. (pin#1,2,3 pin#87-90, TE_Servo: R101, C101) 4) Exchange IC101(AFE). 5) Exchange IC301(MPU & DSP).	No.07
5	47xx	Servo Loop Gain Adjust NG.	47XA: Disc Unmatch(Exchange Disc). 1) Check Pickup FFC Connection. 2) Exchange Pickup (Signal Noisy). 3) Check solder of IC101circumference. (pin#1,2,3 pin#87-90, FE_Servo: R102, C405 TE_Servo: R101, C101) 4) Exchange IC101(AFE). 5) Exchange IC301(MPU & DSP).	No.08
6	49xx	Unwritten Slice Level Adjust NG. (RAM Only)	4906: RAM Disc NG (Exchange Disc). 1) Check solder of IC101circumference. (pin#1,2,3 pin#87-90) 2) Exchange IC101(AFE). 3) Exchange IC301(MPU & DSP).	N0.09

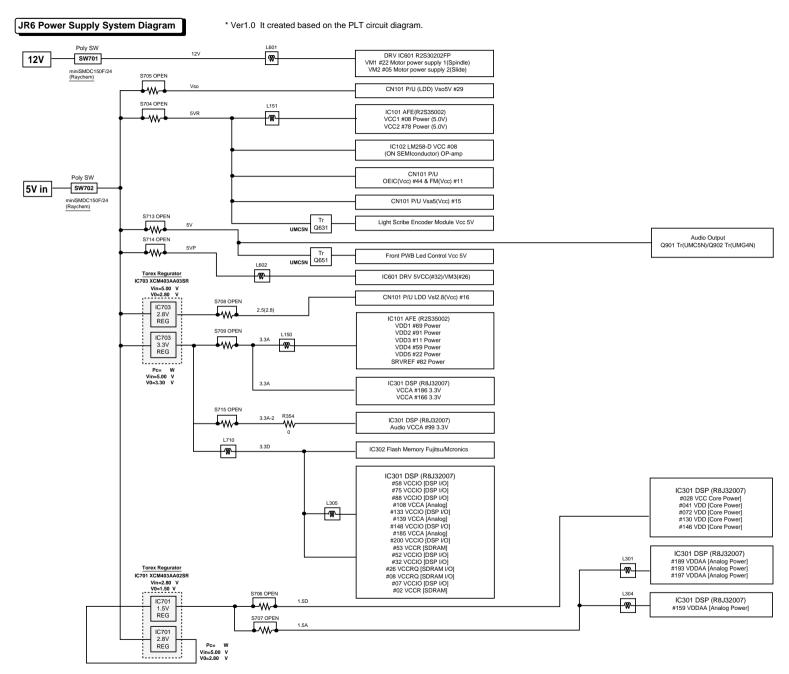
No.	Error Code SSB Byte21,22	Contents of fail	Fail Analysis	Block Diagram
7	4Axx	Focus Offset Adjust NG. (DVD-ROM,CD-R/RW)	4A08: Disc Unmatch(Exchange Disc). 1) Check Pickup FFC Connection. 2) Exchange Pickup. 3) Exchange IC301(MPU & DSP).	No.10
8	4A5x 4A6x	Focus Offset Adjust NG. (RAM Only for PID)	1) RAM Disc NG (Exchange RAM Disc) 2) Exchange Pickup 3) Exchange IC101(AFE) 4) Exchange IC301(MPU & DSP)	No.11
9	4A8x	Focus Offset Adjust NG. (RAM Only for Data)	4A88: RAM Disc NG (Exchange RAM Disc). 1) Exchange Pickup. 2) Exchange IC101(AFE). 3) Exchange IC301(MPU & DSP)	No.12
10	4B0x	Tilt Adjust NG(RAM Only).	1) Check Pickup FFC Connection. 2) Exchange Pickup. 3) Check solder of IC101circumference. (pin#6,7 R106, C106, R107, C107) 4) Exchange IC101(AFE). 5) Exchange IC301(MPU & DSP).	No.13
11	4B8x	Tilt Adjust NG(DVD-/+ R/RW).	1) Check Pickup FFC Connection. 2) Exchange Pickup. 3) Check solder of IC601 circumference. 4) Exchange IC601. 5) Check solder of IC301 circumference. 6) Exchange IC301 7) Exchange Slider Motor.	No.14
12	4CCx	Data Slice Adjust NG. (RAM Only)	1) Exchange Pickup. 2) Exchange IC101(AFE). 3) Exchange IC301(MPU & DSP).	No.12
13	4Dxx	Focus Deviation Adjust NG.	1) Check Pickup FFC Connection. 2) Exchange Pickup. 3) Check solder of IC301circumference. 4) Exchange IC301(MPU & DSP).	No.15
14	182x 01xx	Home Position Adjust NG. (DVD-SL Only)	Check FFC Connection. Check Slider FPC Connection. Exchange Slider Motor. Check solder of IC101circumference. Exchange IC101(AFE).	No.21
15	52xx	Focus Offset Adjust NG. (DVD-R/RW, +R/RW)	1) Check Pickup FFC Connection. 2) Exchange Pickup. 3) Check solder of IC101circumference. (pin#1,2,3 pin#87-90, TE_Servo: R101, C101) 4) Exchange IC101(AFE).	No.16

No.	Error Code SSB Byte21,22	Contents of fail	Fail Analysis	Block Diagram
16	54xx	DPP Amp Adjust NG. (CD Disc Only)	1) Check Pickup FFC Connection. 2) Exchange Pickup. 3) Check solder of IC101circumference. (pin#1,2,3 pin#87-90, TE_Servo: R101, C101) 4) Exchange IC101(AFE). 5) Exchange IC301(MPU & DSP).	No.07
17	55xx	Lens Shift/ Tilt Adjust NG. (CD Disc Only)	Check Pickup FFC Connection. Exchange Pickup. Check solder of IC601 circumference. Exchange IC601. Check solder of IC301 circumference. Exchange IC301 Exchange IC301 Exchange Slider Motor	No.14
18	56xx	Focus Level Adjust NG.	1) Check Pickup FFC Connection. 2) Exchange Pickup. 3) Check solder of IC101circumference. (pin#1,2,3 pin#87-90, PE_Servo: R103, C406) 4) Exchange IC101(AFE). 5) Exchange IC301(MPU & DSP).	No.06
19	57xx	HFPE Amp/Gain Adjust NG.	1) Check Pickup FFC Connection. 2) Exchange Pickup. 3) Check solder of IC101circumference. (pin#6,7 R106, C106, R107, C107) 4) Exchange IC101(AFE). 5) Exchange IC301(MPU & DSP).	No.13
20	58xx	Lens Sensitivity Adjust NG.	1) Check Pickup FFC Connection. 2) Exchange Pickup. 3) Check solder of IC301circumference. 4) Exchange IC301(MPU & DSP).	No.17
21	59xx	Spindle Offset Adjust NG.	1) Check Spindle FFC Connection. 2) Check solder of IC601circumference. (pin#12-14) 3) Exchange IC601(Driver). 4) Exchange Spindle Motor. 5) Check solder of IC301circumference. 6) Exchange IC301(MPU & DSP).	No.18

No.	Error Code SSB Byte21,22	Contents of fail	Fail Analysis	Block Diagram
22	5Axx	ADIP read timing Adjust NG.	5A01: Check DVD+R Disc (Exchange Disc) . 1) Check Pickup FFC Connection. 2) Exchange Pickup. 3) Exchange IC101(AFE). 4) Exchange IC301(MPU & DSP). 5) Exchange IC601(Driver)	No.19
23	5Cxx	Signal Amp Error.	1) Check Pickup FFC Connection. 2) Exchange Pickup. 3) Check solder of IC101circumference. (pin#1,2,3 pin#87-90, PE_Servo: R103, C406) 4) Exchange IC101(AFE). 5) Exchange IC301(MPU & DSP).	No.06
24	5Dxx	Focus Offset Adjust NG. (DVD-R/RW,+R/RW in Data)	1) Check Pickup FFC Connection. 2) Exchange Pickup. 3) Check solder of IC101circumference. 4) Exchange IC101. 5) Check solder of IC701circumference. 6) Exchange IC301(MPU & DSP). 7) Exchange Slider Motor.	No.20

3. Loading Sequence Error (Lead in Error)

No.	Error Code SSB Byte21,22	Contents of fail	Fail Analysis	Block Diagram
1	2503,2504	RTZ Timeout(Sled Timeout).	1) Check Slider FPC Connection. 2) Check solder of IC601 circumference . (pin#2-3, 6, 8-10) 3) Exchange IC601. 4) Exchange Slider Motor.	No.21
2	2020,2021	Focus Fail.	 Check Pickup FFC Connection. Exchange Pickup. Check solder of IC601circumference. Exchange IC601(Driver) Check solder of IC101circumference. (pin#1,2,3pin#87-90, FE_Servo: R102, C405) Exchange IC101(AFE). 	No.22
3	2101,2102	Tracking Fail.	 Check Pickup FFC Connection. Exchange Pickup. Check solder of IC601circumference. Exchange IC601(Driver). Check solder of IC101circumference. (pin#1,2,3 pin#87-90, TE_Servo: R101, C101). Exchange IC101(AFE). 	No.22
4	2000~2010	Spindle Fail.	1) Check Spindle FFC Connection. 2) Check solder of IC601circumference. (pin#12-14) 3) Exchange IC601(Driver). 4) Exchange Spindle Motor. 5) Check solder of IC301circumference. 6) Exchange IC301(MPU & DSP).	No.18



PCB Poor Analysis - Check list

1 Power supply Line-12V 12V CN801-41 2 Line-5V 5V CN801-44 3 (IC701) reg-1.5V 1.5V IC701-2 4 reg-2.8V 2.8V IC703-5 5 (IC703) reg-3.3V 3.3V IC703-2 6 Flash-ROM VDD: 3.3V 3.3V 37 7 (IC302) CS Active-Low 26 8 XRD read-CK 28 9 DSP VDD: 1.5V 1.5V 41, 28, 72, 130, 146, 159, 189, 193, 197	185,
3 (IC701) reg-1.5V 1.5V IC701-2 4 reg-2.8V 2.8V IC703-5 5 (IC703) reg-3.3V 3.3V IC703-2 6 Flash-ROM (IC302) VDD: 3.3V 3.3V 37 7 (IC302) CS Active-Low XRD 26 XRD read-CK 28	185,
4 reg-2.8V 2.8V IC703-5 5 (IC703) reg-3.3V 3.3V IC703-2 6 Flash-ROM VDD: 3.3V 3.3V 37 7 (IC302) CS Active-Low 26 8 XRD read-CK 28	185,
5 (IC703) reg-3.3V 3.3V IC703-2 6 Flash-ROM VDD: 3.3V 3.3V 37 7 (IC302) CS Active-Low 26 8 XRD read-CK 28	185,
6 Flash-ROM VDD: 3.3V 3.7 7 (IC302) CS Active-Low 26 XRD read-CK 28	185,
7 (IC302) CS Active-Low 26 XRD read-CK 28	185,
8 XRD read-CK 28	185,
	185,
9 DSP VDD: 1.5V 1.5V 41, 28, 72, 130, 146, 159, 189, 193, 197	185,
	185,
10 (IC301) VCC(D): 3.3V 3.3V 7, 32, 52, 58, 75, 88, 133, 148, 200, 199, 2, 53,	
139, 108, 8, 26	
11 VCC(A): 3.3V 3.3V 186, 166, 99	
12 Clock-34MHz 33.8688MHz 106, 107	
13 MRSTB (3.3V)High 202	
14 AFE VCC: 5.0V 5.0V 8, 78	
15 (IC101) VDD : 3.3V 22, 11, 91, 59, 69, 82	
16 OP-amp VCC : 5.0V 5.0V 8	
(IC102)	
17 7ch-DRV 5VCC: 5V 5V 32	
18 (IC601) VM3 : 5V 26	
19 VM1, 2 : 12V 12V 5, 22	
20 REF: 1.65V 1.65V 42	
21 Pick-up VCC(FM): 5.0V 5.0V 11	
22 VCC(OEIC) : 5.0V 5.0V 44	
23 VC(OEIC) : 2.1V 2.1V 43	
24 VREF: 2.5V 2.5V 9	
25 VSL25 : 2.8V 2.8V 16	
26 VSA5 : 5.0V 5.0V 15	
27 VSO: 5.0V 29	

 $^{^{\}star}$ When there are twe or more power supply pins of LSI, it checks by one ramdom pin first.

HW Self- Diagnostic function

1. Self-Diagnostic Function by LED Blink.

- Basic operation: At JR6, MPU is included in DSP, MPU accesses each peripheral (inside, exterior) device, and discover a defect by the ability of a read/write of data to be performed correctly. Since MPU operates by the program with a built-in Flash-ROM, when abnormalities are in MPU, Flash-ROM, and these Data-Bus & control signals, this self-diagnostic function cannot be used. In such a case, the case where LED does not light up at all at the time of a power supply injection is almost the case.
- MPU: In DSP Flash-ROM (16Mb) is connected to the exterior Bus of MPU. Even if the MPU-Bus terminal of
 Flash-ROM short-circuits, it becomes impossible for MPU to read the right program data from Flash-ROM,
 and stops for this reason, turning on LED at all. On the other hand, the own poor device of DSP, and the
 open state of IC-pin, when a defect does not influencing Bas of MPU, it can detect correctly and becomes
 blink of LED according to those defects.
- **DSP**: DSP has ATAPI-IF, LDD-serial-IF, AFE-serial-IF, and an AFE control signal as Digital-IF. As Analog-IF, it has the slice circuit of RF signal from AFE, PLL, the objects ADC and DAC for SERVO, and ADC for ADIP detection. Among these, own poor Digital of DSP, and AFE-serial-IF can detect by this self-diagnostic function.
- AFE: Poor detection of AFE is restricted to detection of a limitation-item. Since the greater part of the function is analog signal processing, AFE serves as a register in AFE, and a check, which accepts it, serial IF in the logical digital examination from MPU. In addition, serial-IF for AFE control is performed via DSP. This is writing in the Write command and setting data, and is automatically transmitted to the predetermined register of DSP. Conversely, when it leads the register information on AFE, the read command can be written in the predetermined register of DSP, and the value of an AFE register can be read by reading the read register of DSP after that. Therefore, serial [between the poor register of AFE, and AFE and DSP], when there is LED blink with poor AFE the defect of IF or the defect of the register for AFE of DSP is considered.
- Refer to the contrast table of the number of times of blink of LED, and a poor part.
- The self-diagnostic function by this LED blink is carried out in the state of a set without a PCB independent or loading Disc.

- 2. LED does not blink at all at the time of a power supply injection. Eject-SW does not react.
- (1) Is it normal to the exterior Bus (Data-Bus, Address-Bus, control signal system) of MPU? Viewing check: -- a short circuit, opening, etc.

. The device connected to the exterior Bus of MPU in DSP, and its signal list

Peripheral device	Flash -ROM
[Bus/Signal]	(IC302)
Address	A1~A20
Data	D0~D15
CS*	CS0B
WCK	WR
RCK	RD

^{=&}gt; It repairs, when abnormalities are discovered.

(2) Does the power supply circuit operate normally?

External input 12V, external input 5V, regulator 3.3V, regulator 2.8V, and regulator 1.5V

- =>When the abnormalities are discovered, an external power supply, a power supply cable, and Regulator IC are exchanged.
- => Since a problem is in a load side when not improving, even if it exchanges the above, and attached sheet JR6 power-supply system figure is made reference, and poor portions, such as a short circuit of a power supply part, are found out and fixed.

(3) Is the clock of MPU in DSP oscillated correctly?

Checked the ceramic oscillation element's X301 both-ends and DSP(106)(107) 33.87MHz oscillating.

=> When 3.3V power supply is correctly supplied to DSP and the clock is not oscillating correctly, it is the defect of MPU, or an oscillation element defect, and part exchange is performed in order of DSP and X301.

(4) The defect of Flash-ROM

Although the clock of DSP is oscillating correctly and the power supply circuit is also outputting normal voltage, when LED does not blink at all at the time of a power supply injection and Eject-SW does not react, either, poor Flash-ROM is the most doubtful.

=> Flash-ROM (IC302) are exchanged.

Note: Before Flash-ROM exchange, the CS signals of the external device of MPU in DSP connection, an Address signal, and a Data signal are observed on a waveform level, and since the but most amount of work and the special knowledge which can raise the discovery accuracy of a poor part are necessities, recommendation is impossible.

- (5) Even if it performs the above-mentioned repair, when not improving, the disconnection and the short circuit which cannot be discovered, can be considered in viewing of PCB. Moreover, partial breakage (although a clock is oscillated, somewhere in insides do not operate.) of DSP can be considered.
 - => When not improving above, the possibility that a PCB pattern is faulty is high, and judges repair to be difficult.

3. Motor, Abnormalities in Actuator System

The drive circuit of a motor & actuator consists of the three ICs IC601(R2S30202FP). The work of each IC is as follows.

(1) IC601(R2S30202FP): 7ch driver

Spindle motor driver: 180° audio drive Type, an analog input, a PWM drive, a Vm=12V.

Stepping motor driver X2: analog input, a PWM drive (differential), a Vm=12V

Loading motor driver: Input/Output PWM drive, Vm=5V.

Focus actuator driver: analog input / output (differential), a Vm=5V Tracking actuator driver: analog input / output (differential), Vm=5V Tilt actuator driver: analog input/output (differential), Vm=5V.

A motor & actuator and its correspondence pin

Signal/CH	SPDL-MT	STEP-MT	Load-MT	Focus-ACT	Track-ACT	Tilt-ACT
Input	(1)SPIN	(2)SL1IN (3)SL2IN	(41)LOIN	(40)FOIN	(39)TOIN	(38)TLIN
Reference	(42)REF 1.65V					
Output	(12)U (13)V (14)W	(6)SL2+ (8)SL2- (9)SL1+ (10)SL1-	(27)LO+ (28)LO-	(34)FO+ (35)FO-	(31)TO+ (30)TO-	(36)TL+ (37)TL-

A control mode setup by the control terminal

EN1(20)	EN2(21)	SPDL	SLED	Load	Focus/Track/Tilt
Low	Low	off	off	off	off
Low	High	off	on	on	off
High	Low	on	on	off	on
High	High	on	on	off	on

